Technical Manual for DVC's DigitEyes Cameras

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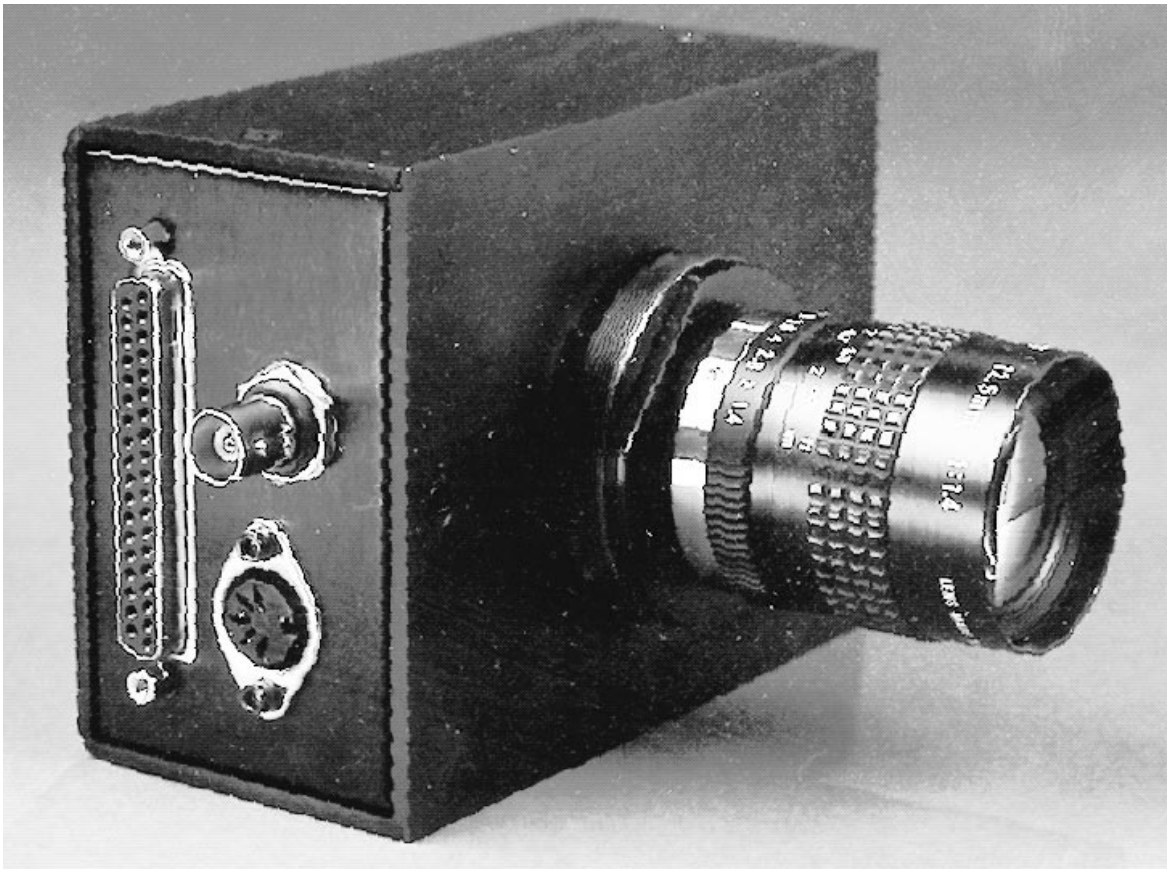

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1. Introduction:

DVC Company, a San Diego, California based manufacturer of cost-effective, rugged video cameras, thanks you for purchasing from the “DigitEyes" series of digital and analog video cameras.

This series of cameras is based on the premise that to-day's high-end image processing applications DEMAND cameras that are designed for the maximum accuracy and repeatability that can be achieved with to-day's CCDs. DVC's moderately priced cameras occupy a niche BETWEEN the low-end "security and surveillance" cameras which are inexpensive but inaccurate, and the expensive, non real-time, high resolution cameras that might be "overkill" for many applications.

The 30 frames/sec video data is provided as 10 or 8 bit parallel, differential RS-422 data which is "plug-and-play" compatible with industry-standard image processors and a simultaneous RS-170 composite video signal (Signal-to-Noise ratio ≥62 dB @ 0.5 lux, 100 IRE). The digital data, pixel clock, enable line, enable frame and field index signals are accessible via DB-37 connector. Manual (or remote) external gain / offset or Automatic Gain Control (AGC) functions that can provide nearly 30 dB of gain are available with the RS-170 output to "tune" the dynamic range of the camera to the application. This provides an optimum match between the dynamic range & sensitivity of the camera and the requirements of the application - in some cases, optimum imagery is obtained under low-light conditions in real time (30 frames per second) without an external image intensifier !

The TC-245 CCD imager has a 755(H) X 484(V) interlaced image format and has on-chip correlated clamp sample & hold circuitry that minimizes noise. The CCD has a full well of >80,000 electrons and a noise floor of <30 electrons (at 25°C). It has no "dead" pixels or "blemishes" that are found in low-end security and surveillance CCD cameras.

The CCD is physically mounted in a cavity within a high-precision opto-mechanical plate to eliminate the stability problems that are caused by using imprecisely aligned cameras in high-end applications. On-camera digitization using the CCD pixel clock eliminates pixel jitter, improves repeatability and brings sub-pixel accuracy to image processing applications.

The DVC-0A (analog only RS-170 model) is upgradeable to the DVC-08 or DVC-10 models which are 8 or 10 bit digital RS-422 cameras with simultaneous RS-170 output. The camera can, literally, "grow" with your application ! Shuttering, Pulse driven integration, cooling to -25°C, genlock (for multiple camera synchronization, removal of the sensor faceplate for UV applications are options that are available upon request. All DVC cameras come with a standard 2 year warranty and use industry-standard C-mount lenses.

In today's state-of-the-art digital video applications, the parallel 8 or 10 bit digital data can be serialized and transmitted via fiber optic cable or over other channels. This is achievable without any degradation of the signal quality over long distances.

This manual applies to all three of the DigitEyes cameras. Since the Analog Video Output is common to all three cameras, any reference to the Analog Video Output applies equally to all three cameras. References to the Digital Video Output applies only to the DVC-08 and DVC-10 cameras.

2. CAMERA SPECIFICATIONS:

2.1 OPTICAL

Optical Filtering	IR filter (optional; see Figure 2-1 & 2-3)
Spectral Response	See Figure 2-1, 2-2 and 2-3
Sensitivity (without IR filter) @ 2850°K	0.5 Lux (0.05 fc) @ CCD for 100 IRE video (Signal-to-Noise Ratio ≥ 62 dB)

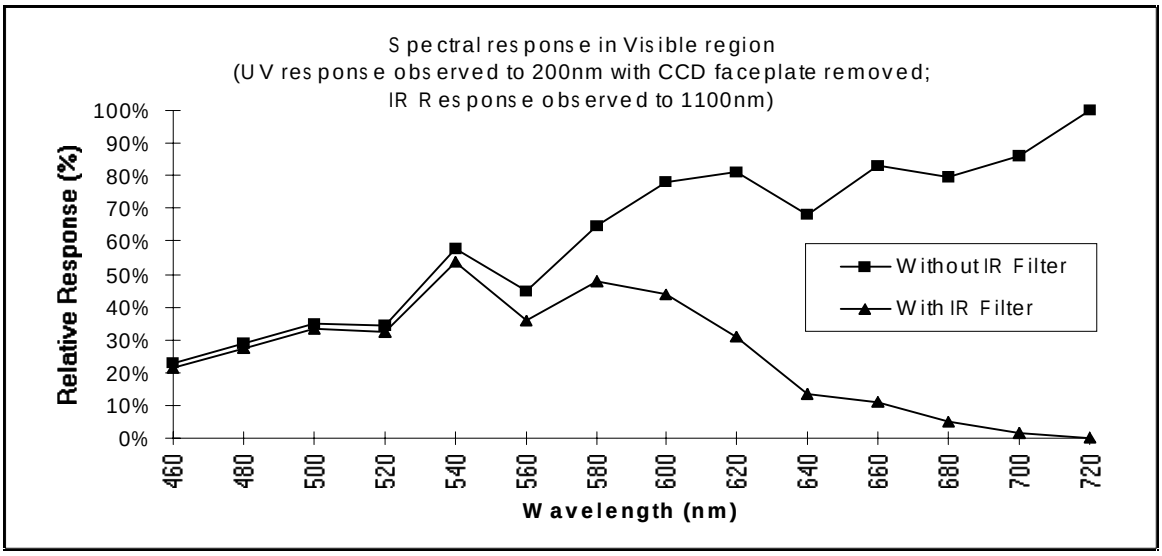

Figure 2-1: Camera Spectral Response

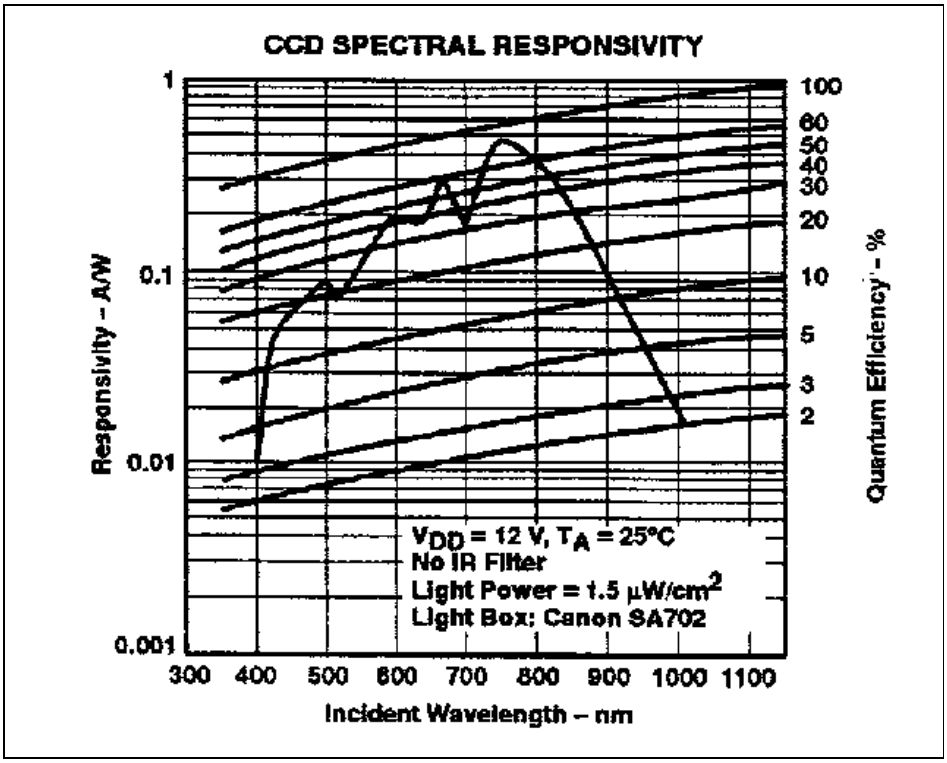

Figure 2-2: TC-245 CCD Spectral Responsivity Curve (© Texas Instruments, 1994)

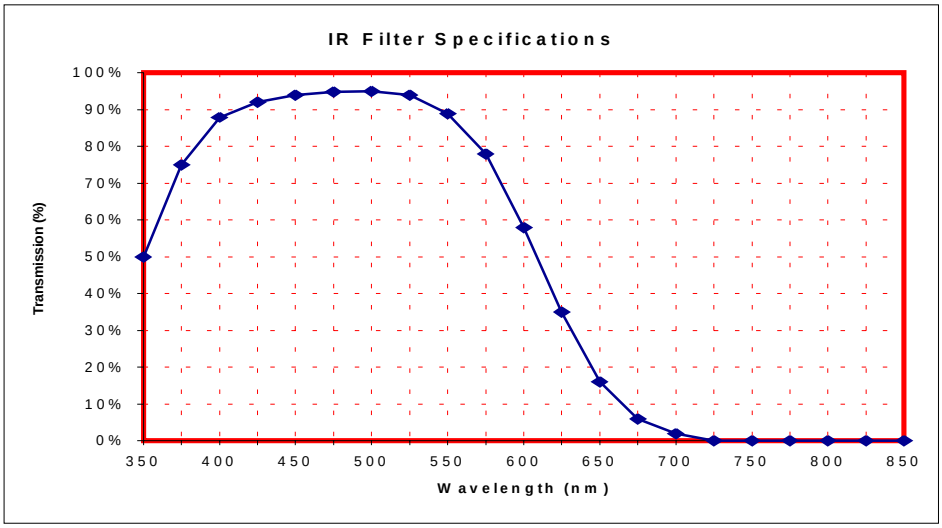

Figure 2-3: IR Filter Characteristics

2.2 DIGITAL VIDEO OUTPUT

Digital Video Output (14.31818 Mbytes/sec)	Ten or Eight bit parallel differential (RS-422)
Gamma	1.0 (linear)
AGC	None

2.3 ANALOG VIDEO OUTPUT

RS-170 Composite Video : 1Vp-p; 75Ω	Resolution: 565 TVL (H); 350 TVL (V)
Gamma (set at the factory)	0.45 (standard); 0.6 (optional); 1.0 (optional)
AGC (set at the factory)	None (standard); 30 dB (optional)
Signal to Noise Ratio (no AGC, Gamma = 1)	≥ 62 dB (See VM-700 plots; Appendix E)

2.4 ELECTRICAL

Timing	RS-170, 2:1 Interlaced
Power Supply Voltages & Current requirements	± 12 V DC each @ 250 mA steady state + 5 V DC @ 250 mA steady state.
Clock Rate	14.31818 MHz
Synchronization	Internal crystal @ 14.31818 MHz
Genlock (Optional)	Reverts to crystal lock w/o External Sync.

2.5 MECHANICAL

Weight (without lens)	1 lb. (approx.)
Temperature limits (operating)	-10°C to 50°C
Temperature limits (storage)	-30°C to 70°C
Dimensions	4¾" X 3¾" X 2½"
Lens mount	Industry standard C- mount
Camera mount	¼ - 20 threaded hole
Digital Video Connector	DB-37, female connector (See Appendix A)
Power Supply Connector	5 pin DIN connector (see Appendix A)
Analog Video Connector	BNC female connector

3. DVC Camera Functional Description

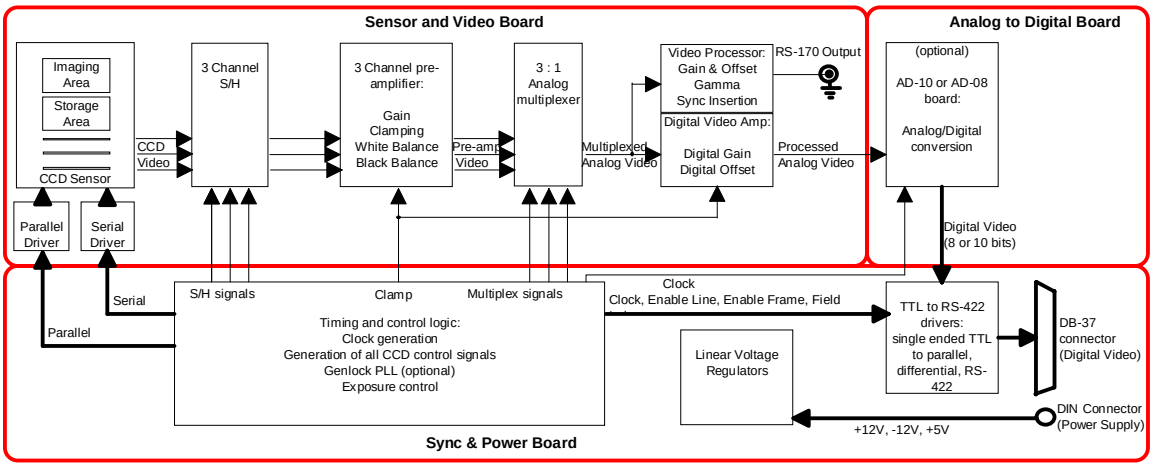

Figure 3-1: Digital Camera Block Diagram

3.1 CCD Sensor:

Light from the scene is brought into focus at the imaging plane of the CCD. An optical block (optional) filters out the IR component of the light.

The following functions take place within the CCD:

3.1.1 Integration:

During the integration period (1/60 sec.), charges are integrated in the active pixel wells of the Imaging Area. The amount of charge that is integrated in each active pixel well is proportional to the illumination received at each active pixel site on the CCD. Anti-blooming pulses during the horizontal and vertical blanking areas trigger the anti-blooming gates that are an integral part of the active pixel elements.

3.1.2 Parallel Transfer:

During the Vertical Blanking interval, the entire charge matrix that was integrated in the previous field (1/60 sec) is shifted to the opaque storage area of the CCD. This is accomplished by a series of 242 pulses, each of which causes the charge matrix to shift down by one line. This process takes approximately 68µsec.

3.1.3 Readout:

In the following field, the charges are transferred from the storage area of the CCD to on-chip serial shift registers and then sequentially to the detection nodes where they are made available as signal voltages. Note: While one field is being read out from the Storage Area, the other field is being integrated in the Imaging Area of the CCD.

3.2 Video Pre-processing:

The low-level video signal voltage from the CCD is fed through a high-speed sample-and-hold amplifier, clamped (for black reference) and amplified before further video processing. It is in

this section that the three channels of video must be "equalized" before they can be multiplexed into a single channel of video. In order to accomplish this, two channels are provided with variable gain and offset; one channel (considered the reference channel) has a fixed gain and offset. The two variable channels are adjusted by means of the White Balance and Black Balance potentiometers until all the three channels are properly matched.

3.3 Analog Video Processing:

The signal from the pre-processor stage is fed to the Video Processor which performs the following functions related to the Analog (RS-170) video:

- Gamma Correction
- Gain and Offset Control
- AGC & Auto-iris (optional)
- Sync Insertion - the Composite Sync signal is added to the Output Video Signal to create Composite Video.
- Video Output Driver - The Video Processor is directly capable of driving a 75Ω co-axial cable. It is recommended that the cable be terminated in its characteristic impedance of 75Ω at the receiving end (the monitor or other receiving device).

3.4 Video Digitization:

The low-level video signal voltage from the pre-processor is clamped (for black reference) and amplified on the Sensor & Video Board before Analog-to-Digital conversion (on the optional Analog to Digital board). The Digital Video Data is latched and converted to an RS-422 format for transmission as a balanced, differential signal along a cable which consists of shielded twisted pairs.

3.5 Sync and Power Board:

This board performs the following functions:

- Voltage Regulation: Input voltages (+12V, -12V and +5V) are converted into several positive and negative voltages required by the CCD and in the video processing circuits.
- Generation of CCD timing signals
- Generation of Video timing signals
- Asynchronous Reset function
- Genlock function
- Electronic Shutter function
- Pulse Driven Integration function
- TTL to RS-422 conversion of digital video data, and all handshaking signals (clock, csync, field index, enable line & enable frame).

4. TC-245 CCD Details

Note: This information has been derived from the Texas Instruments Databook Titled "Area Array Image Sensor Products". ©Texas Instruments 1994

- Frame Transfer CCD Technology. Contiguous pixels for 100% fill factor. No "dead space" between pixels.
- 755 (H) X 242 (V) active picture elements per field.
- Interlaced operation doubles effective vertical resolution; Image format is 755(H) X 484(V)
- 8.5µm (H) X 19.75µm (V) pixel size.
- On-chip correlated-clamp sample & hold circuits to minimize noise.
- On-chip shielded pixels provide "dark pixel" level for black level reference.
- 8 mm. image diagonal, compatible with ½ " optics.
- High sensitivity; unlike Interline Transfer CCDs which have "dead spaces" that lower sensitivity.
- Solid state reliability with no image burn-in, residual imaging, image distortion, lag or microphonics
- Minimum 100:1 blooming overload ratio (with Interlace on).
- 70 dB sensor dynamic range. Full well >80,000 electrons; Noise equivalent signal <30 electrons (typical 20 electrons)
- High photo-response uniformity; <5% photo-response-non-uniformity guaranteed (typical <2%); blemish free sensor.

4.1 TC-245 CCD Functional Details

The TC-245 is a frame transfer charge coupled device (CCD) image sensor designed for use in single chip B/W NTSC TV applications. The device is intended to replace a 1/2 inch vidicon tube in applications requiring small size, high reliability and low cost.

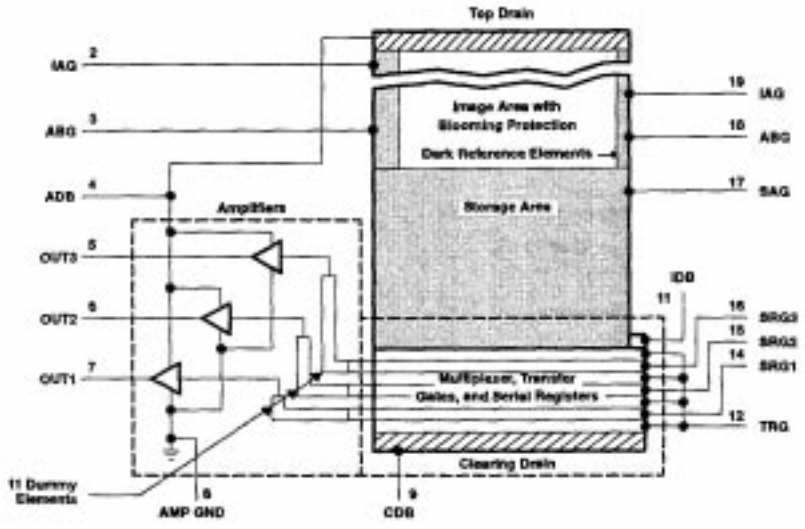

Figure 4-1: TC-245 Block Diagram (© Texas Instruments, 1994)

The Image Sensing area of the TC-245 is configured into 242 lines with 786 elements in each line. 29 elements are provided in each line for dark reference. The blooming protection feature of the sensor is based on recombining excess charge with charge of opposite polarity in the substrate. This Anti-blooming is activated by supplying clocking pulses to the anti-blooming gate, an integral part of each image-sensing element. The sensor is designed to operate in an interlace mode, electronically displacing the image sensing elements in alternate fields by 1/2 of a vertical line during the charge integration period, effectively increasing the vertical resolution and minimizing aliasing. The device can also be operated as a 755(H) X 242(V) non-interlaced sensor with significant reduction in the dark signal.

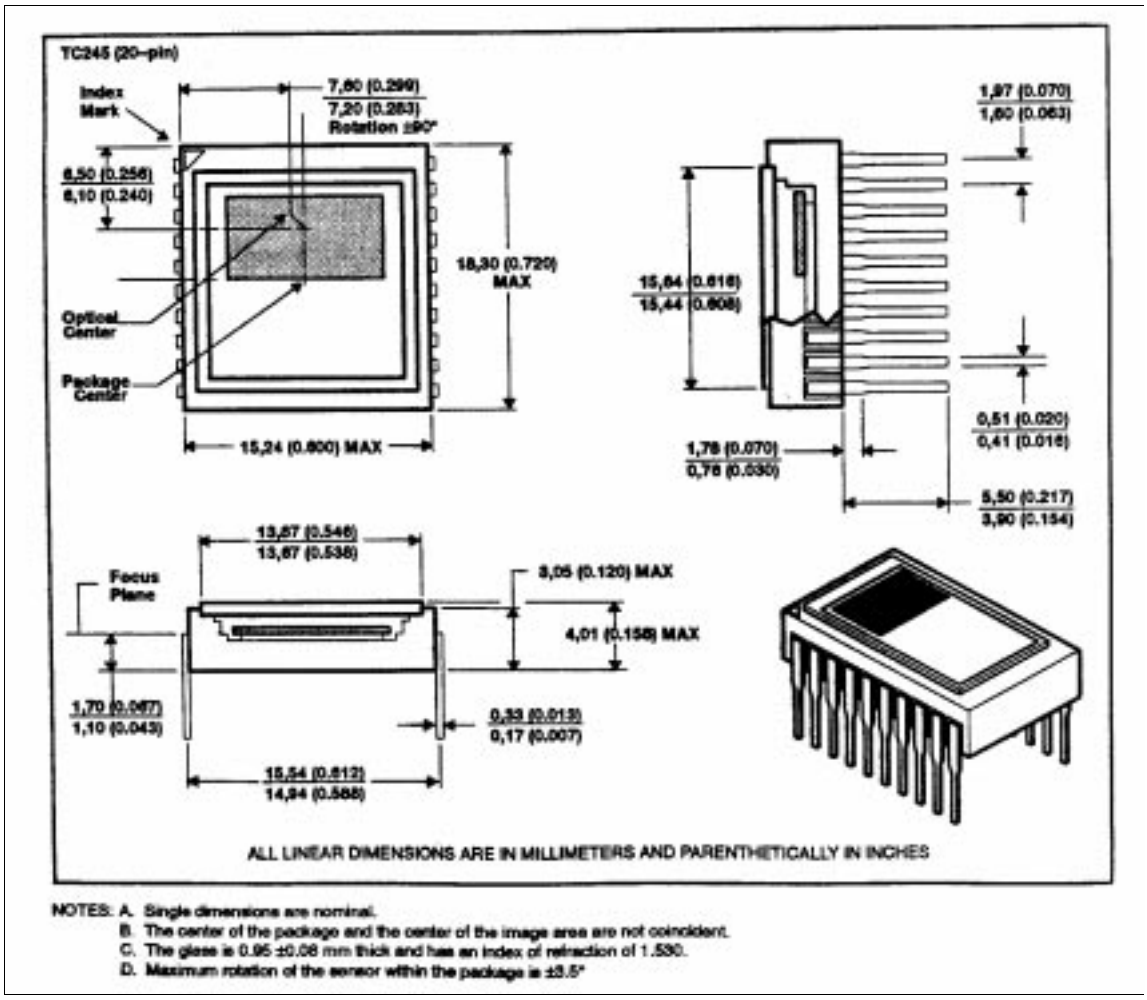

Figure 4-2: TC-245 Mechanical Drawing (© Texas Instruments, 1994)

A gated floating-diffusion detection structure with an automatic reset and voltage reference incorporated on-chip converts charge to signal voltage. The signal is further processed by a low-noise, state-of-the-art correlated clamp-sample-and-hold circuit. A low-noise two-stage, source follower amplifier buffers the output and provides high output drive capability. The image is readout through three outputs, each of which reads out every third image column.

The TC-245 is built using TI-proprietary virtual-phase technology, which provides devices with high blue response, low dark signal, good uniformity and single-phase clocking. The TC-245 is characterized for operation from -10°C to 45°C.

4.2 FUNCTIONAL DESCRIPTION:

The TC-245 consists of four basic functional blocks:

1. Image-sensing area
2. Image-storage area
3. Multiplexer block with serial registers and transfer gates
4. The low-noise signal processing amplifier block with charge detection nodes.

The location of each of these blocks is identified in the functional block diagram.

4.2.1 Image Sensing and Storage Area:

As light enters the silicon in the image sensing area, free electrons are generated and are collected in the potential wells of the sensing elements. During this time, blooming protection is activated by applying a burst of pulses to the anti-blooming gate inputs every horizontal blanking interval. This prevents blooming caused by the spilling of charge from over-exposed elements into neighboring elements. After Integration is complete, the signal charge is transferred into the storage area.

There are 29 1/2 columns of elements at the right edge of the image-sensing area that are shielded from incident light; these elements provide the dark reference used in subsequent video processing circuits to restore the video black level. There are also 1 1/2 columns of light shielded elements at the left edge of the image-sensing area and two lines of light-shielded elements between the image-sensing and image-storage areas (the latter prevent charge leakage from the Image sensing into the Image storage area.

4.2.2 Multiplexer with Transfer Gates and Serial Register:

The Multiplexer and transfer gates transfer charge line-by-line from the storage-area columns into the corresponding serial registers and prepare it for readout. The multiplexer vertically separates the pixels for input into the serial registers. Multiplexing is activated during the horizontal blanking interval by applying appropriate pulses to the transfer gate and the serial registers.

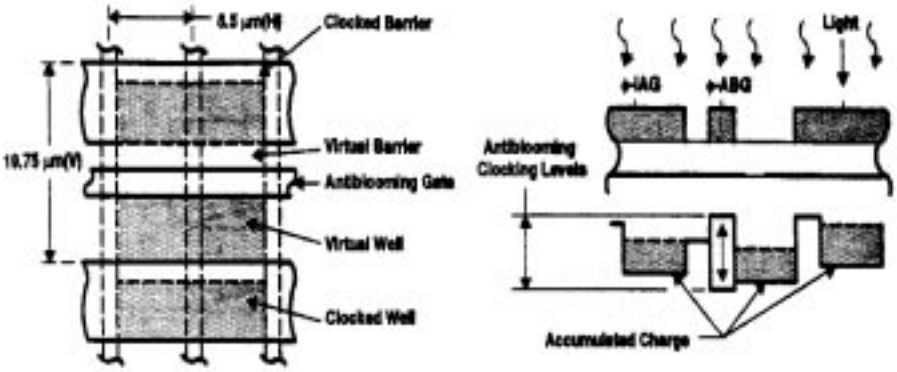

Figure 1. Charge Accumulation Process

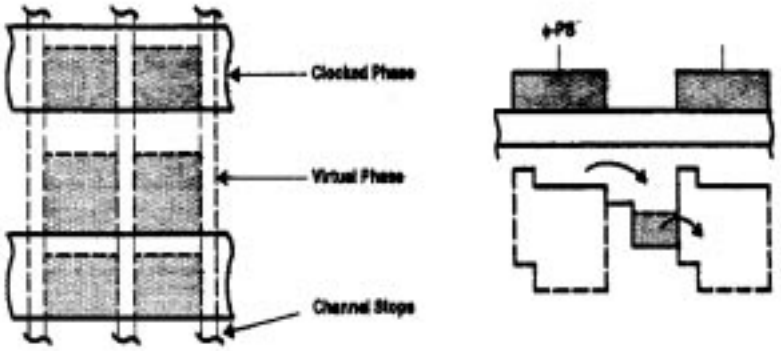

Figure 2. Charge Transfer Process

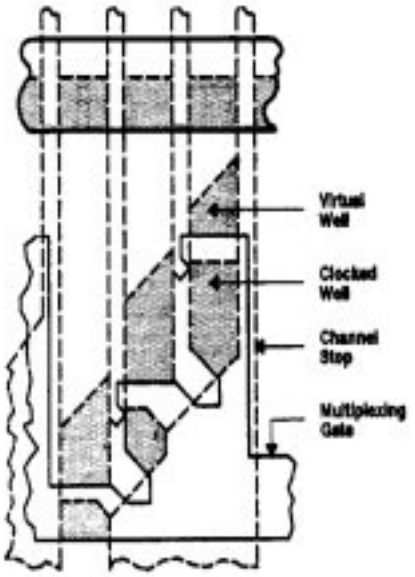

Figure 3. Multiplexing Gate Layout

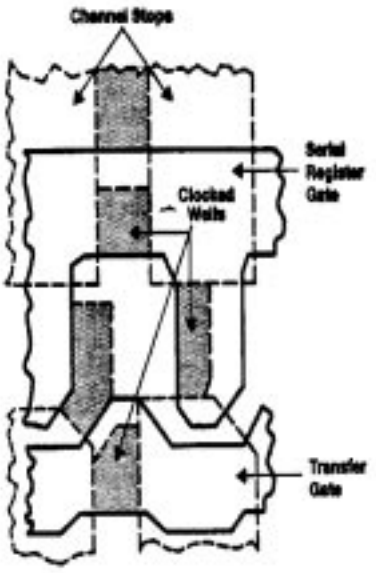

Figure 4. Interface Region Layout

Figure 4-3: TC-245 Gate Level Drawing (© Texas Instruments, 1994)

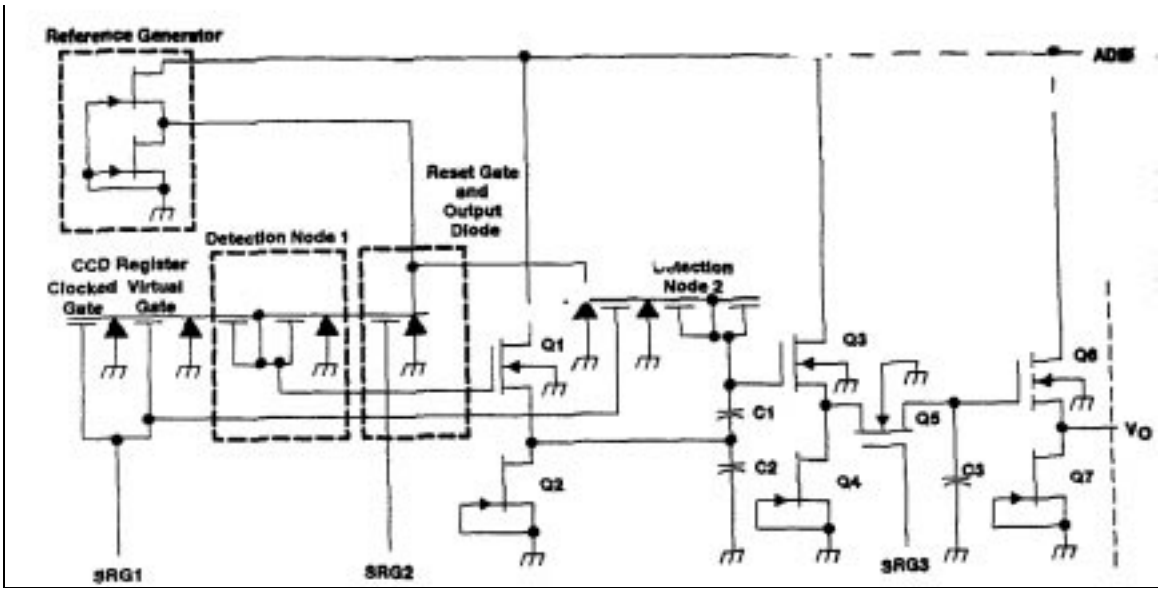

Figure 4-4: TC-245 CCSH Amplifier Circuit (© Texas Instruments, 1994)

4.2.3 Correlated-Clamp-Sample-and-Hold (CCSH) Amplifier with Charge Detection Nodes:

Charge is converted into a video signal by transferring the charge onto a floating diffusion structure in detection node 1 that is connected to the gate of a MOS transistor Q1. The proportional charge-induced signal is then processed by the circuit shown above.

This circuit consists of a low pass filter formed by Q1 and C2, coupling capacitor C1, dummy detection node 2, which restores the DC bias on the gate of Q3, sampling transistor Q5, holding capacitor C3, and output buffer Q6. Transistors Q2, Q4 and Q7 are current sources for each corresponding stage of the amplifier. The parameters of this high-performance signal processing amplifier have been optimized to minimize noise and maximize the video signal.

The signal processing begins with a reset of detection node 1 and a restoration of the DC bias on the gate of transistor Q3 through the clamping function of dummy detection node 2. After the clamping is completed, the new charge packet is transferred onto detection node 1. The resulting signal is sampled by the sampling transistor Q5 and is stored on the holding capacitor C3. This process is repeated periodically and is correlated to the charge transfer in the registers. The correlation is achieved automatically since the same clock lines used in shift registers S2 and S3 for charge transport serve for reset and sample. The multiple use of the clock lines significantly reduces the number of signals required to operate the sensor. The amplifier also contains an internal reference voltage generator that provides the reference bias for the reset and clamp transistors. The detection nodes and the corresponding amplifiers are located some distance away from the edge of the storage area. Therefore 11 dummy elements are incorporated at the end of each serial register to span the distance. The location of the dummy elements, which are considered to be a part of the amplifier is shown in the block diagram.

The above sequence of events helps to remove the noise (called kTc noise) that would otherwise have been introduced due to the "floating" node. By clamping it to a "known" reference between pixel values, and then charging it with the "delta" or the difference of potential due to the new pixel value, a significant source of noise is removed.

5. DVC Camera Options and Special Modifications

- Electronic Shutter (1/1000 sec OR 1/2000 sec)
- Pulse Driven Integration Control
- "N" Field Integration: user specified value of "N"
- Asynchronous Reset Capability
- Genlock Option for multiple camera synchronization
- Gain & Offset Control
- Gamma Correction Options on the Analog Video Output
- Access ports for analog & digital gain/offset as well as for variable gamma control
- External Thermo-electric Cooler
- User Defined Optical Filter
- Board Level Cameras (for OEMs)
- Silicon Graphics Inc (SGI) INDY & INDIGO2 Digital Compatibility - Call DVC for an update !
- Electronically tunable (350nm to 1100nm) solid state LCD filter with fast switching for sequential RGB and other multi-spectral applications; Call DVC for info !
- Serial Digital Video (for transmission via fiber optic, RF or twin co-ax)

5.1 TYPICAL MODE CONTROL TABLES

Some typical examples of mode control tables are shown the the next two sections. The actual table in a particular camera depends upon the combination of options that are ordered. Note: since the Mode Control 1 (MC1 or DB37-pin37) and the Mode Control 0 (MC0 or DB37-pin18) are often used for the external analog video gain and offset control voltages, units that have these external options selected are limited in the number of exposure control options that are provided. In some cases, a special auxillary connector may be provided on the camera side panel to increase the number of "mode control" inputs.

5.1.1 "N" Field Integration, Pulse Driven Integration & Asynchronous Reset :

DB37 - 19	DB37 -37		
MC2	**MC1**	**Mode**	**Reset**
0	0	Normal (Default: 1/60sec, Integ. period = 16.66ms)	↓ edge
0	1	"N" Field Integ. (N = 60); Integ. period = 1 second	inactive
1	0	Pulse driven integ. (Reset LOW sets Integ. period)	¯|___|¯
1	1	Normal (Default: 1/60sec, Integ. period = 16.66ms)	↓ edge

Since all Mode Control (MC) and RESET pins are internally pulled up, the unit defaults to the normal (1/60sec) mode until a pin is pulled LOW (via a computer, or by connecting it to ground).

Note: If a remote control box (with mode selection) is plugged in, the switch position should be set to "NORMAL" before any of the Mode control pins is pulled LOW (via the DB37 connector) by a computer or an external device other than the remote control box.

5.1.2 "N" Field Integration; 4 values of "N", Two-speed Electronic Shutter, Pulse Driven Integration & Asynchronous Reset:

DB-37 pins				
19	37	18		
MC2	MC1	MC0	Mode	Reset pin 17
0	0	0	"N" Field Integration (N = 2) Integ. period = 33.33ms	inactive
0	0	1	"N" Field Integration (N = 4) Integ. period = 66.66ms	inactive
0	1	0	"N" Field Integration (N = 6) Integ. period = 99.99ms	inactive
0	1	1	"N" Field Integration (N = 12) Integ. period = 199.99ms	inactive
1	0	0	Shutter (1/1000 sec, Integration period = 1.0ms)	inactive
1	0	1	Shutter (1/2000 sec, Integration period = 0.5ms)	↓ edge
1	1	0	Pulse driven integ. (Reset duration sets Integ. period)	‾|___|‾
1	1	1	Normal (Default: 1/60sec, Integration period = 16.66ms)	↓ edge

Since all Mode Control (MC) and RESET pins are internally pulled up, the unit defaults to the normal (1/60sec) mode until a pin is pulled LOW (via a computer, or by connecting it to ground).

5.2 ELECTRONIC SHUTTERING MODE:

For integration periods less than 1/1000 sec, the following process (called electronic shuttering) is carried out.

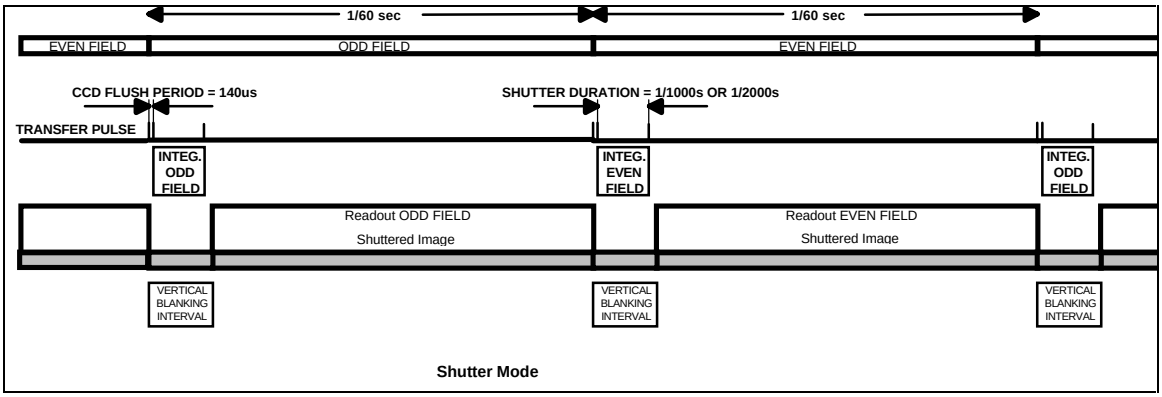

Figure 5-1: Shutter Mode Timing Diagram

At the beginning of the Vertical Blanking Interval, the CCD is flushed by means of two charge transfers. This takes approximately 140µsec. After the two "clearing" transfers, the Integration Period begins. Before the end of the Vertical Blanking Interval, however, a "readout" transfer takes place. The period between the two clearing transfers and the third (readout) transfer is the Integration Period; it's duration is dependent on the user selected speed of the shutter (1/1000 sec or 1/2000 sec).

The following active field is used to read out the charge that was integrated in the Imaging Area during the Integration Period. By completing the entire Integration Period within the Vertical Blanking Interval, the electronic shuttering process can be done without disturbing the normal sync and timing of the camera.

Since the pseudo-interlacing is enabled during this mode, two distinct fields are obtained. For a stationary object in the field-of-view, this produces two interlaced fields; or full vertical resolution. Since the two integration periods are 1/60 sec apart, any movement in the field-of-view between the two integration periods will be seen as inter-field flicker.

Therefore, if shuttering is used to "stop" motion, only one field (or half the normal vertical resolution) per integration period is usable. If shuttering is used for exposure control and the field-of-view is static (relative to the 1/60 sec between successive exposures), full vertical resolution is available.

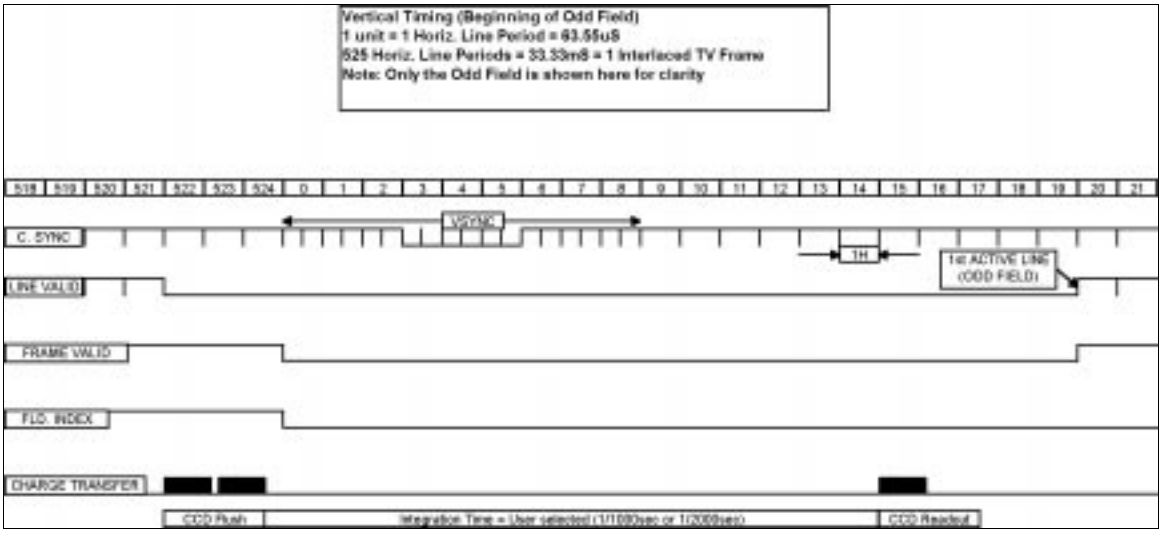

Figure 5-2: Shutter Mode Details (Vertical Blanking Interval)

Both the Genlock and the Asynchronous Reset options have been found to work successfully with the shutter mode, although the “slowest” shutter speed obtainable with Genlock or Asunchronous Reset is approximately 600µsec (instead of 1/1000 sec).

5.3 PULSE DRIVEN INTEGRATION MODE:

For integration periods greater than 1/1000 sec, the following process (called Pulse Driven Integration) is followed. The camera operates in the standard mode (Integration Period = 1/60 sec) as long as all the mode control pins are High. Due to internal pull-up resistors, this is the default mode.

If the Integration mode is selected (see mode selection table), then the falling edge of the RESET input (pin 17 of the DB-37 connector) signal initiates the INTEGRATION MODE sequence.

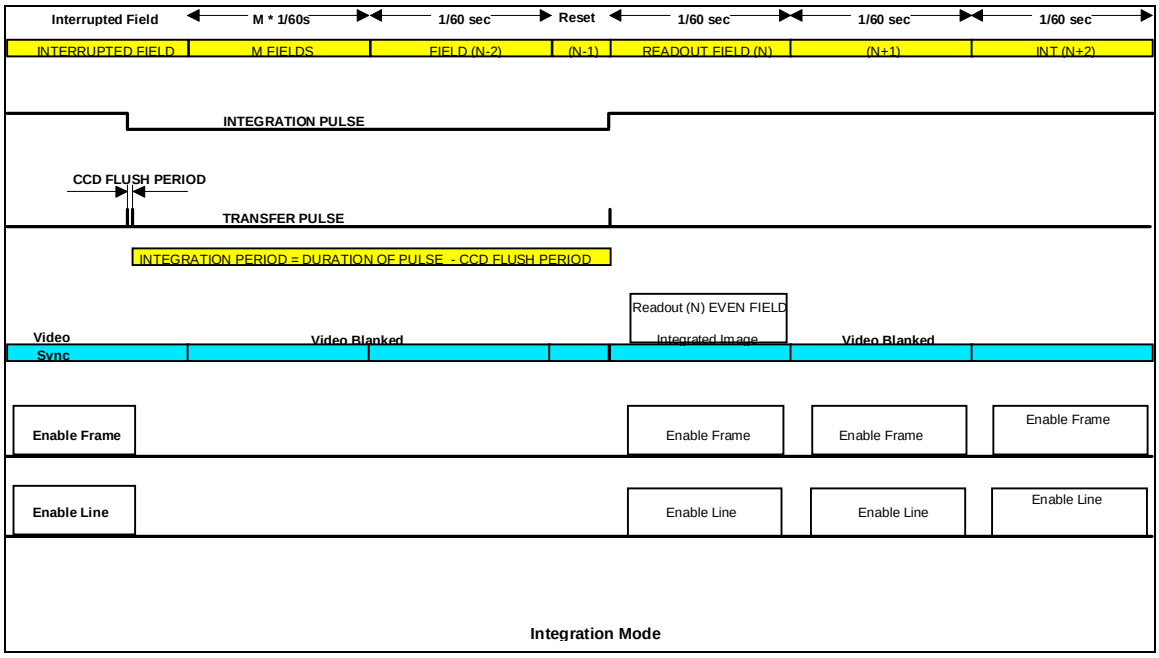

Figure 5-3: Pulse Driven Integration Mode

The CCD is flushed by means of two quick, successive transfers. This takes approximately 140µsec. At the end of this period, the Integration Period begins.

When the RESET signal returns HIGH (rising edge), a vertical reset is generated. This resets the Vertical Counter in the Camera; image transfer and readout begin immediately.

The total integration time is therefore can be computed as follows:

T_{int} = (Duration of the Low RESET pulse) - (CCD flush period)

OR

T_{int} = (Duration of the Low RESET pulse) - 140µsec

Note(s):

(1) Only one field (or half the normal vertical resolution) per integration period is obtained.

(2) Since charge transfer is initiated only when the RESET pulse is asserted (LOW), there is no image generated by the camera except the one field due to each INTEGRATION sequence.Therefore the monitor screen remains blank, until the next INTEGRATION sequence is initiated by the next falling edge of RESET.

(3) The Pulse Driven Integration mode is designed for applications where the user has complete control of the integration period. When the Pulse Driven Integration mode is selected (using the Mode Control bits), the CCD does NOT integrate charge until the RESET pulse is asserted LOW. Therefore, as long as RESET is HIGH, the camera does NOT produce an image. However, clock and sync. are generated, so that a frame grabber (or image processor) can be in synchronization with the camera. The Enable Frame and Enable Line signals are also generated. Since the camera does not produce an image while it is waiting for an active LOW RESET pulse, any frames of video data that are captured (or viewed on a monitor) during this waiting period will be black.

(4) When the RESET pulse transitions (HIGH to LOW) the CCD is flushed (cleared of charge) by means of two quick, successive charge transfers. As soon as the CCD is flushed, the active integration period begins. This period lasts as long as the RESET pulse is LOW. During this period, the Enable Frame and Enable Line signals are NOT asserted, since no active video is being generated while the integration takes place.

(5) When the RESET pulse transitions (LOW to HIGH) the final “readout” transfer takes place. The timing chip is also reset to line 6 of the ODD field (simultaneous to the readout transfer in the CCD). Active video is output starting at line 20 (standard RS-170 format). The Enable Frame and Enable Line signals are generated, beginning at line 20. This is the image of the scene that was integrated on the CCD during the LOW duration of the RESET pulse.

(6) There is no lower or upper theoretical limit to the integration period. In reality, the upper limit is determined by the amount of noise that can be tolerated and the dynamic range required by the application. The lower limit is determined by the amount of light during image transfer and the amount of smear that can be tolerated by the application. Cooling the CCD will result in longer usable integration periods due to a reduction in the dark current of the CCD.

5.4 N FIELD INTEGRATION:

If the N Field Integration mode is selected, the following sequence is followed.

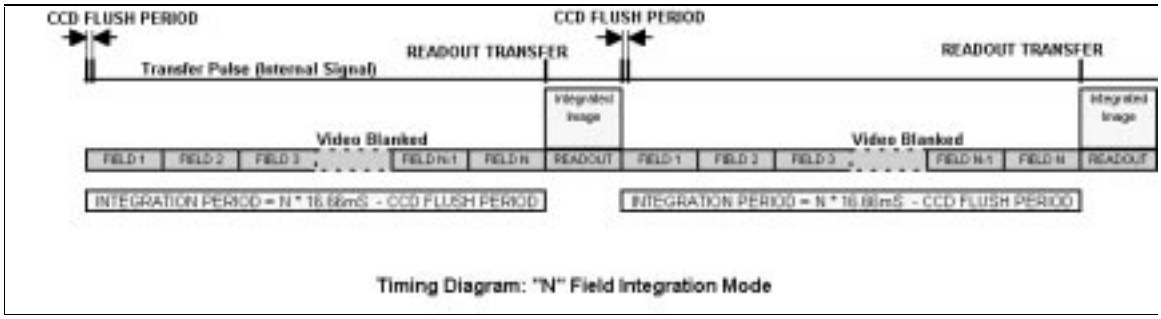

Figure 5-4: "N" Field Integration Mode

The CCD is flushed by means of two quick, successive transfers. This takes approximately 140μsec. At the end of this period, the Integration Period begins.

The Integration Period has a duration of N fields; image transfer and readout begin immediately.

The total integration time is therefore can be computed as follows:

T_{int} = N * (16.66mS) - (CCD flush period)

Where N is the number of fields during which charge is accumulated on the CCD.

For N = 6, the nominal integration period is 6 * 16.66mS = 99.99mS.

More accurately (for N = 6),

T_{int} = 99.99mS - 140μsec

Note (1): Only one field (or half the normal vertical resolution) per integration period is obtained.

Note (2): Since charge transfer is initiated only at the end of the N Field integration period (before the readout field), there is no image generated by the camera except during the one Readout field due to each INTEGRATION sequence. Therefore the video output is blanked, until the next Readout field.

Note (3): There is no theoretical upper limit to the integration period. In reality, the upper limit is determined by the amount of noise that can be tolerated and the dynamic range required by the application. The lower limit is determined by the amount of light during image transfer and the amount of smear that can be tolerated by the application. Cooling the CCD will result in longer usable integration periods due to a reduction in the dark current of the CCD.

5.5 Asynchronous Reset and Genlock

5.5.1 Standard Mode:

The standard mode of operation results from an internally generated clock which is derived from an internal crystal oscillator. The frame rate of 30 Hz is independent of any external event.

In some applications, it is necessary to synchronize the camera to external events. Two methods are available:

1. Asynchronous Reset: Synchronizes the camera to an external asynchronous reset pulse
2. Genlock: Synchronizes the camera to an external source of Composite Sync OR Video

5.5.2 Asynchronous Reset Mode:

The camera operates in the standard mode as long as the RESET (DB-37 connector, pin 17) is High. Due to an internal pull-up resistor, this is the default mode.

A falling edge of the RESET input signal initiates the ASYNCHRONOUS RESET sequence. An internal circuit detects the falling edge (the duration of the RESET pulse is not significant) and resets the Vertical Counter (to the top of the ODD field) in the Camera. A frame transfer and normal readout of the interrupted field ensue and a new integration on the CCD commences. If no further RESETS occur, normal operation is resumed. It is the responsibility of the application to ensure that the RESET is synchronized properly with the event that is to be viewed.

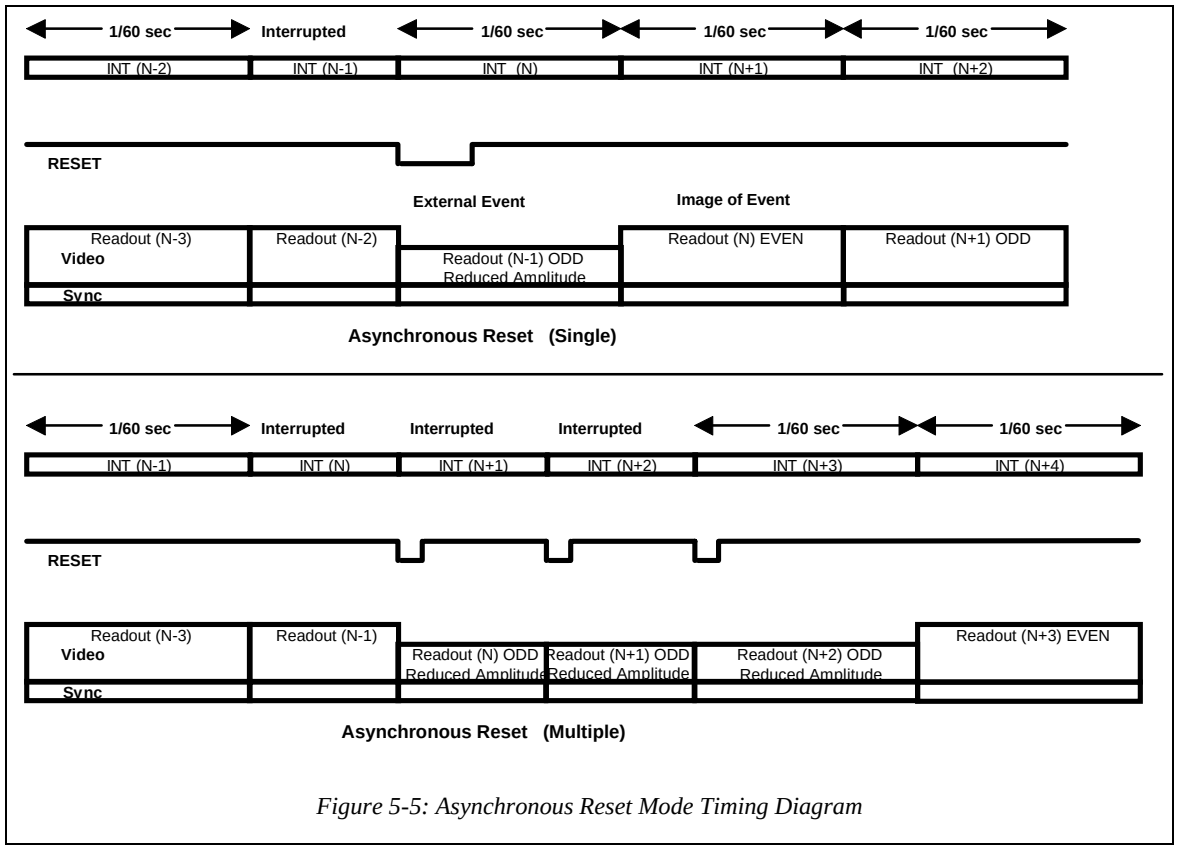

Figure 5-5: Asynchronous Reset Mode Timing Diagram

5.5.2.1 Asynchronous Reset and Shutter:

The ASYNCHRONOUS RESET option has been found to work successfully with Shutter option.

5.5.2.2 Video Amplitude in Asynchronous Reset Mode:

The readout following the interrupted field will have a video amplitude that is proportionally lower than the standard video amplitude, due to a shorter integration period.

5.5.2.3 Multiple Resets per Field (higher "field" rate):

If multiple resets occur within a single field period (1/60 sec), the camera outputs a sequence of partial, ODD fields with reduced video amplitudes. A standard monitor will be unable to lock to this kind of video signal ! A frame grabber may be required to acquire and display this sequence of images. The effect of this operation will be to generate partial fields at a fast "rep rate". This mode may be useful for some Motion Analysis applications.

5.5.3 Genlock Mode:

The camera operates in the standard mode until a CSYNC or ANALOG VIDEO signal is fed into the genlock input (Note: this input is available on cameras specially modified for the GENLOCK option). Within a few milli-seconds the Phase-Locked Loop within the camera "locks" to the incoming CSYNC or ANALOG VIDEO signal. Both the Digital and Analog Video outputs are now locked to the incoming signal.

This mode is sometimes used to lock several cameras together. One approach to this is to use one camera as a "master" source of VIDEO and to lock several "slave" cameras to the master VIDEO. Another approach is to operate all cameras as "slaves" to an external source of CSYNC or VIDEO. Both approaches have been used successfully.

5.5.3.1 Genlock and Shutter:

The GENLOCK option has been found to work successfully with the Shutter option.

5.6 GAIN AND OFFSET

5.6.1 Standard Configuration:

In the standard configuration, the analog video gain/offset and the digital video gain/offset are optimized, for good image quality. User access of these adjustments is possible removing the cover of the camera and adjusting potentiometers on the video board. As a special modification, access to these potentiometers may be provided through holes in the camera cover; contact DVC for details.

The following options affect only the Analog Video on DVC-0A, DVC-08 and DVC-10 cameras. For information on Digital Video gain / offset control, see Frequently Asked Questions !

5.6.2 Manual External Gain Control:

If this option is installed, the internal analog gain control potentiometer is replaced by an external multi-turn potentiometer that is installed on an external "black box". The potentiometer circuit connects to the camera through the DB-37 connector (pin 37 is used for the gain control DC voltage). Since power is derived from the camera AUX. POWER pin (DB-37, pin 36), no external power supply is needed. A micrometer knob with a locking mechanism allows the user to accurately calibrate the application and lock-in an optimum gain setting for the application's light level. The range of operation of the External Gain function is approximately 26 dB, from a maximum of 43 dB to a minimum of 17 dB. It has a linear response (see curve below).

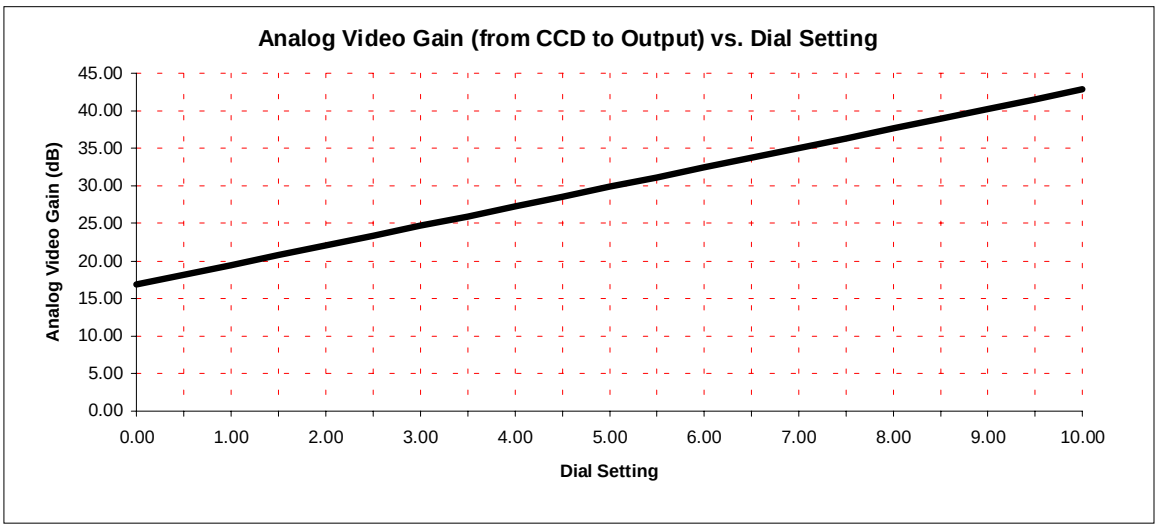

Figure 5-6: Manual External Gain Control Curve

5.6.2.1 Gain vs. Noise:

The increase of gain increases the noise that is present on the video signal; the signal-to-noise ratio of the analog video signal is considerably degraded in low-light, high gain situations. However, some scientific applications benefit greatly from the EGC function. Since DVC cameras have much higher signal-to-noise ratios than average analog video cameras, they produce much less noise (even in low-light, high gain situations) than most competing products.

5.6.2.2 Default:

The camera defaults to max. gain if the external "black box" is not plugged into a camera that has been modified for EGC.

5.6.3 Manual External Offset Control:

If this option is installed, the internal analog offset control potentiometer is replaced by an external multi-turn potentiometer that is installed on an external "black box". The potentiometer circuit connects to the camera through the DB-37 connector (pin 18 is used for the offset control DC voltage). Since power is derived from the camera AUX. POWER pin (DB-37, pin 36), no external power supply is needed. A micrometer knob with a locking mechanism allows the user to accurately calibrate the application and lock-in an optimum offset setting for the application's light level. The range of operation of the External Offset function is 0 to 14 IRE units from a dial setting of 0.00 to 10.00 respectively. It has a linear response (see curve below).

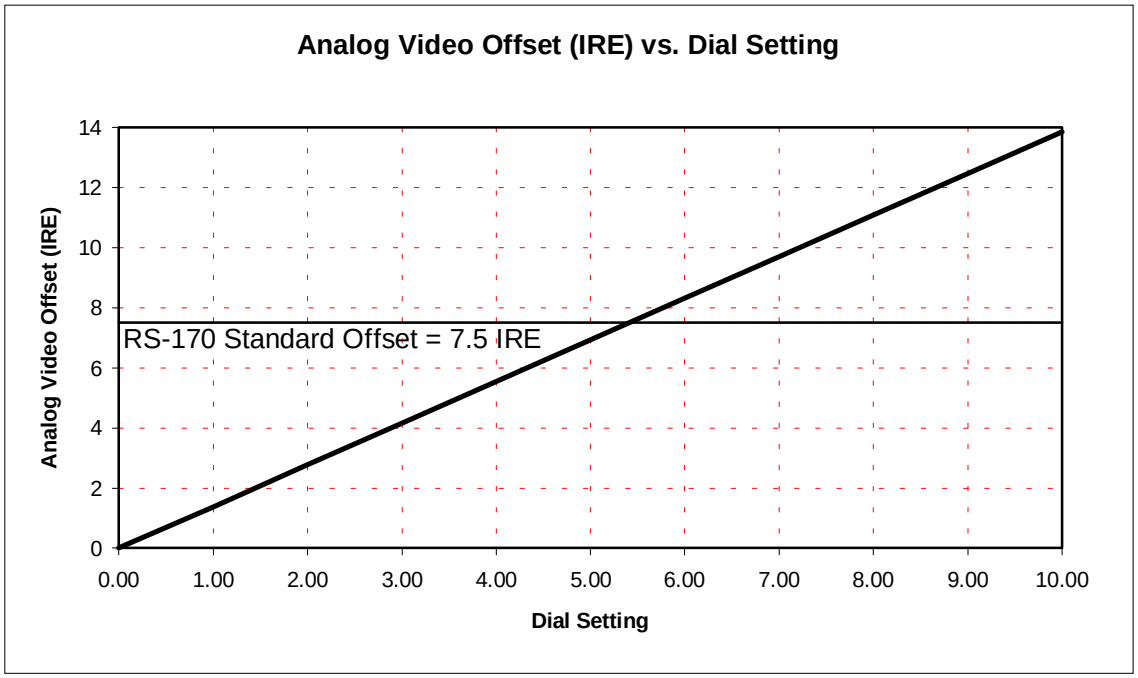

Figure 5-7: Manual External Offset Control Curve

5.6.3.1 Default:

The camera defaults to max. offset if the external "black box" is not plugged into a camera that has been modified for External Offset Control.

5.6.3.2 RS-170 Pedestal:

The RS-170 standard specifies a "setup" or "pedestal" of 7.5 IRE units. As shown on the above curve, this is obtained with a micrometer dial setting of around 5.25 (actual settings will vary slightly from unit to unit).

5.6.4 Computer Driven External Gain Control:

If this option is installed, the internal analog gain control potentiometer is removed and the gain control function may be performed by feeding a variable DC voltage to the camera via DB-37 connector (pin 37). This control voltage may be generated from any external source, including (but not limited to) a Digital-to-Analog converter on an Image Processor or computer peripheral board. The range of operation of the External Gain function is determined by the range of control of the video processing circuit and is approximately 26 dB, from a maximum of 43 dB (at 2V) to a minimum of 17 dB (at 4V). It has a linear response between 2V and 4V but flattens out below 2V and above 4V (see curve below). Yes, the negative slope is real and NOT a typo !

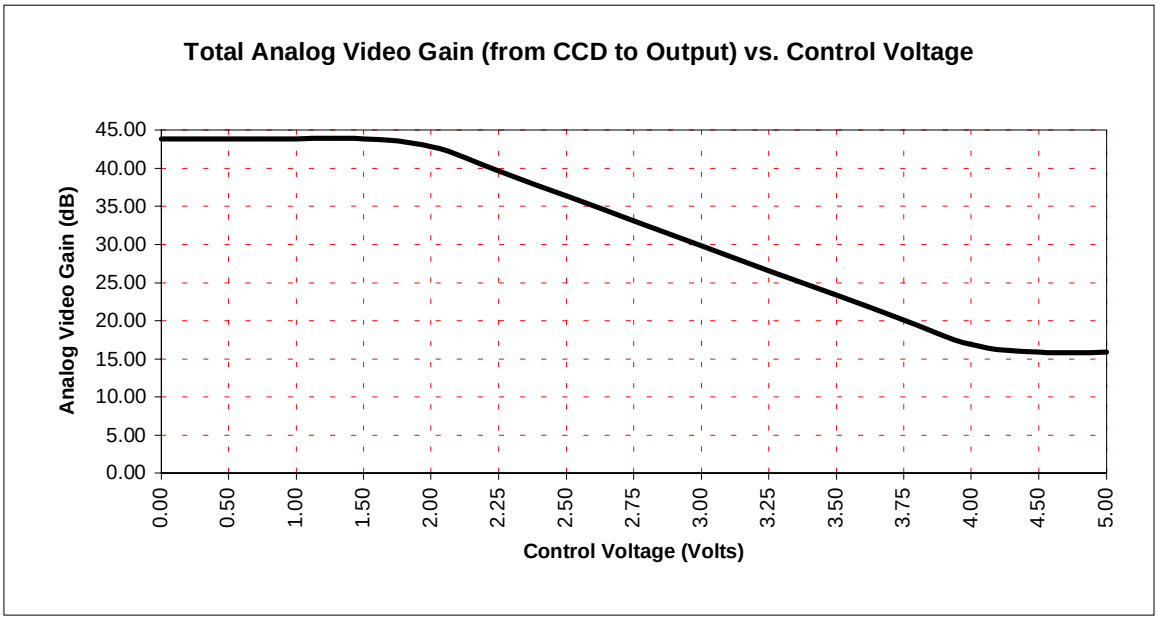

Figure 5-8: External Gain Control Curve

5.6.4.1 Gain vs. Noise:

The increase of gain increases the noise that is present on the video signal; the signal-to-noise ratio of the analog video signal is considerably degraded in low-light, high gain situations. However, some scientific applications benefit greatly from this function. Since DVC cameras have much higher signal-to-noise ratios than average analog video cameras, they produce much less noise (even in low-light, high gain situations) than most competing products.

5.6.4.2 Default:

The camera defaults to max. gain if an external voltage source is not plugged into a camera that has been modified for External Gain Control.

5.6.5 Computer Driven External Offset Control:

If this option is installed, the internal analog offset control potentiometer is removed and the offset control function is performed by feeding a variable DC voltage to the camera via DB-37 connector (pin 18 is used for the offset control DC voltage). This control voltage may be generated from any external source, including (but not limited to) a Digital-to-Analog converter on an Image Processor or computer peripheral board. The range of operation of the External Offset function is 0 to 14 IRE units from 2V to 3.125V respectively. It has a linear response between 2V and 3.125V (see curve below).

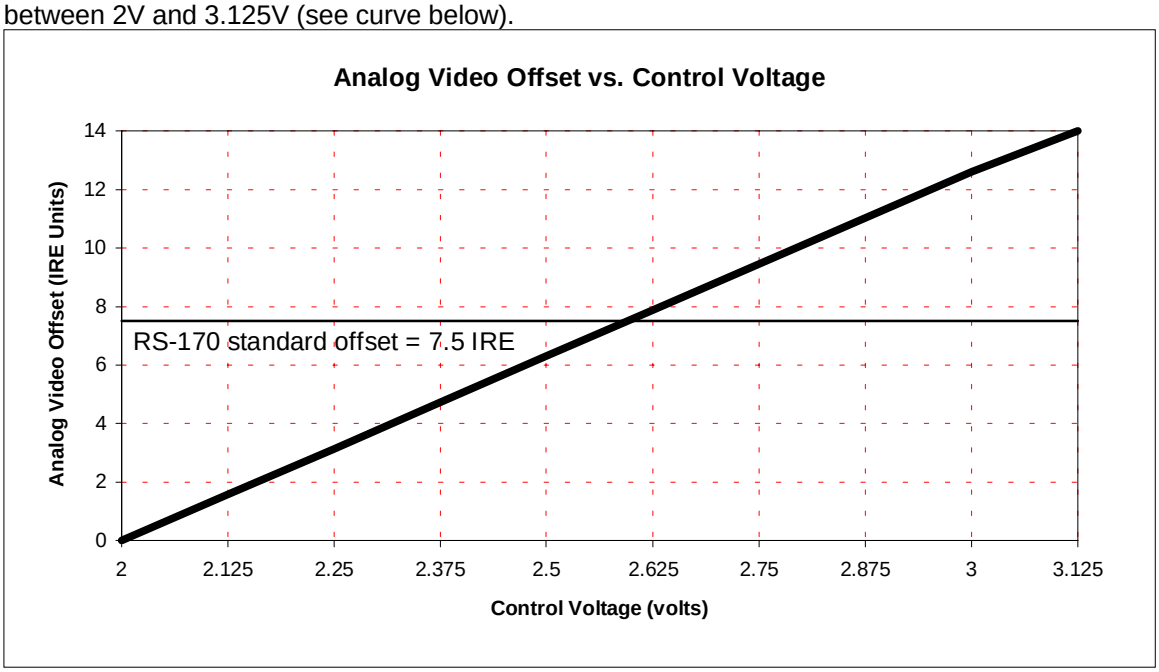

Figure 5-9: External Offset Control Curve

5.6.5.1 Default:

The camera defaults to max. offset if the external "black box" is not plugged into a camera that has been modified for External Offset Control.

5.6.5.2 Linear Range of Control:

Care should be taken to keep the control voltage in the linear range between 2V and 3.125V; outside this range, the offset defaults to certain "preset" levels in a discontinuous manner !

5.6.5.3 RS-170 Pedestal:

The RS-170 standard specifies a "setup" or "pedestal" of 7.5 IRE units. As shown on the above curve, this is obtained with a control voltage of around 2.6V (actual settings will vary slightly from unit to unit).

5.6.6 Automatic Gain Control (AGC):

If this option is installed, the analog video output signal level is maintained at a preset (80 IRE) level even if the ambient scene illumination varies. This is achieved by a feedback loop which senses the average video output level and electronically controls the gain of the video processing circuit to maintain the preset level of output video. The range of operation of the AGC function is determined by the range of control of the video processing circuit and is approximately 26 dB. It has a linear response.

5.6.6.1 AGC and Auto-Iris:

The range of automatic response of the camera to changes in ambient light can be extended with the use of the Auto-Iris option. If this option is installed, it works in tandem with the AGC function. As the scene illumination is decreased, the Auto-Iris lens "opens" wider until it reaches it's maximum - after that, any decrease in scene illumination results in an increase of AGC gain.

5.6.6.2 AGC and Noise:

The increase of AGC gain increases the noise that is present on the video signal; the signal-to-noise ratio of the analog video signal is considerably degraded in low-light, high gain situations. However, some applications benefit greatly from the AGC and Auto-Iris functions. Since DVC cameras have much higher signal-to-noise ratios than average analog video cameras, they produce much less noise (even in low-light, high gain situations) than most competing products.

5.6.6.3 Automatic OR Manual Gain:

"Automatic" controls, such as AGC and Auto-Iris, are usually not suitable in applications where absolute measurements are being made. If gain control is desired in such applications, the manual OR computer controlled external gain control options are usually preferred.

5.7 REMOTE CONTROL BOX:

If the external analog gain & offset control options are installed in a camera, a special remote control box may be connected to the DB-37 connector of the camera via a cable.

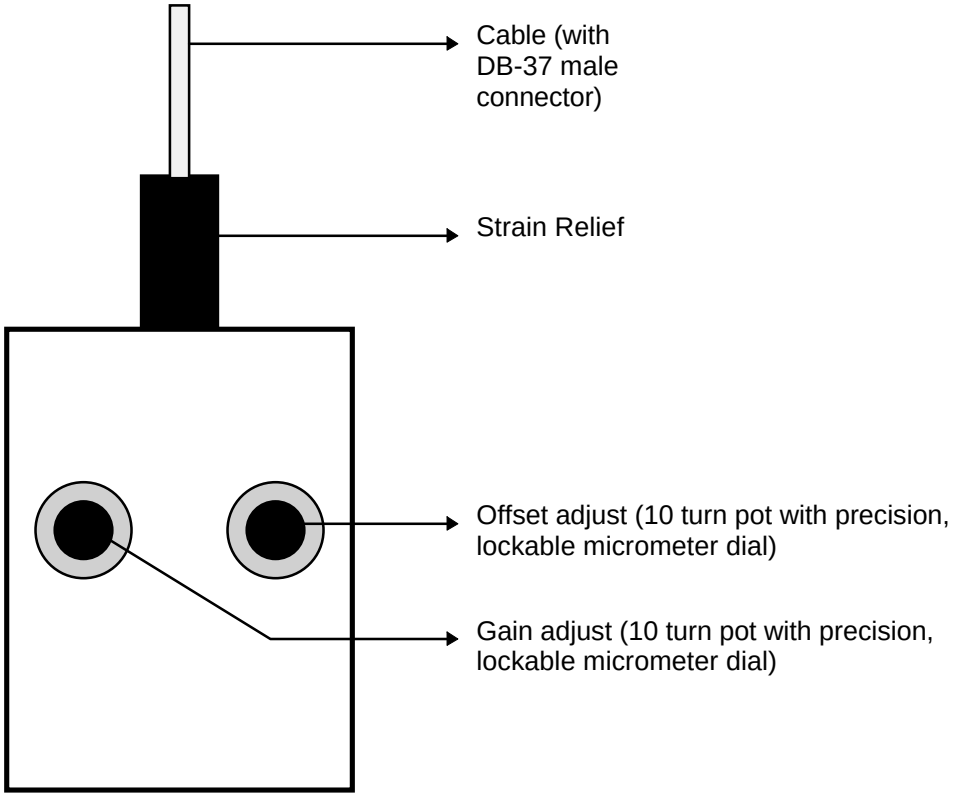

Figure 5-10: Remote Control Box (Top View)

Note: In some cases, a two or three position (and sometimes an eight position knob-switch) is also installed on the remote control box. This allows mode selection via the Remote Control box.

In other cases, a “Y” cable may be needed to connect a camera simultaneously to a remote control box AND the digital port of a Frame Grabber or Image Processor (within a PC).

5.8 Custom Cable Splitter ("Y" cable):

This is a custom cable (often referred to as a Y-cable or a T-cable) that is used in applications where it is necessary to access the DB-37 connector of a DVC "DigitEyes" camera (DVC-0A, DVC-08 or DVC-10) camera at two separate interfaces.

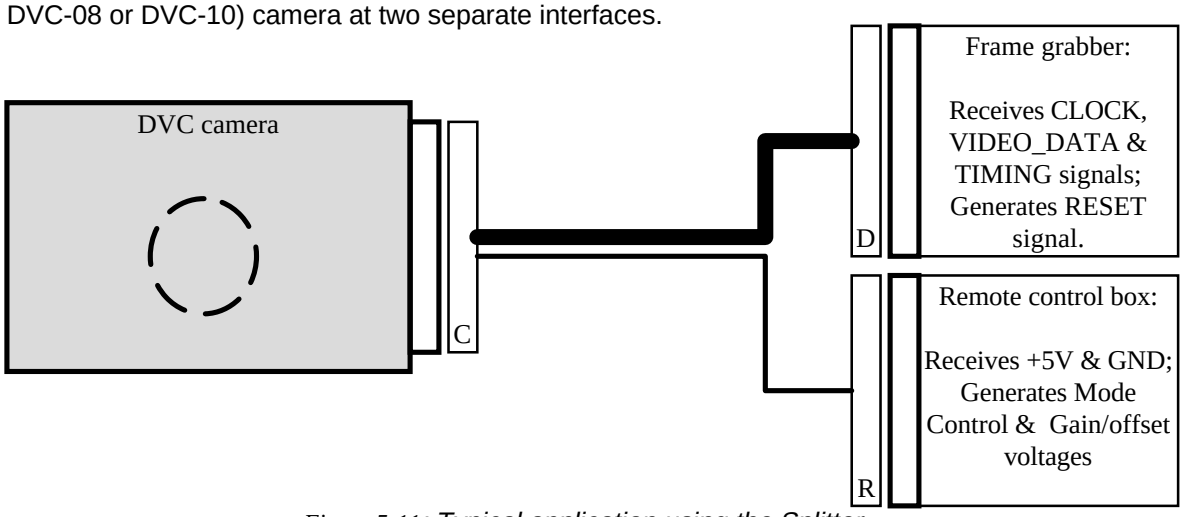

Figure 5-11: Typical application using the Splitter

PIN	SIGNAL NAME	PIN	SIGNAL NAME
1	PIXEL CLOCK (+)	20	PIXEL CLOCK (-)
2	LINE DATA VALID (+)	21	LINE DATA VALID (-)
3	FRAME DATA VALID (+)	22	FRAME DATA VALID (-)
4	COMPOSITE SYNC (+)	23	COMPOSITE SYNC (-)
5	FIELD INDEX (+)	24	FIELD INDEX (-)
6	VIDEO DB9 (+) (LSB FOR DVC-10)	25	VIDEO DB9 (-) (LSB FOR DVC-10)
7	VIDEO DB8 (+)	26	VIDEO DB8 (-)
8	VIDEO DB7 (+) (LSB FOR DVC-08)	27	VIDEO DB7 (-) (LSB FOR DVC-08)
9	VIDEO DB6 (+)	28	VIDEO DB6 (-)
10	VIDEO DB5 (+)	29	VIDEO DB5 (-)
11	VIDEO DB4 (+)	30	VIDEO DB4 (-)
12	VIDEO DB3 (+)	31	VIDEO DB3 (-)
13	VIDEO DB2 (+)	32	VIDEO DB2 (-)
14	VIDEO DB1 (+)	33	VIDEO DB1 (-)
15	VIDEO DB0 (+) MSB	34	VIDEO DB0 (-) MSB
16	GROUND	35	GROUND
17	RESET	36	+5VOLT AUX. POWER OUT
18	MODE CONTROL 0 (Or Offset Control)	37	MODE CONTROL 1 (Or Gain Control)
19	MODE CONTROL 2		

Table 5-1: "Y" Cable: Pinout of camera side DB-37 connector (marked "C")

The splitter connects to the female DB-37 connector (see Table 1, above) of the camera via a male DB-37 connector from which TWO branches emerge.

(1) The Mode Control branch: consisting of the Mode Control signals, which, in the case of MC1 and MC0 may be used as the gain and offset control voltages if the ext. gain/offset option is installed.

Note: The Reset input signal (pin 17) is brought out on both branches of the splitter cable. This allows the generation of the Reset signal from the Frame Grabber OR an external source. Only one source may drive the Reset input at any given time !

PIN	SIGNAL NAME	PIN	SIGNAL NAME
1		20	
2		21	
3		22	
4		23	
5		24	
6		25	
7		26	
8		27	
9		28	
10		29	
11		30	
12		31	
13		32	
14		33	
15		34	
16	GROUND	35	GROUND
17	RESET	36	+5VOLT AUX. POWER OUT
18	MODE CONTROL 0 (Or Offset Control)	37	MODE CONTROL 1 (Or Gain Control)
19	MODE CONTROL 2		

Table 5-2: "Y" Cable: Pinout of Remote box DB-37 connector (marked "R")

(2) The Digital Signals branch:

PIN	SIGNAL NAME	PIN	SIGNAL NAME
1	PIXEL CLOCK (+)	20	PIXEL CLOCK (-)
2	LINE DATA VALID (+)	21	LINE DATA VALID (-)
3	FRAME DATA VALID (+)	22	FRAME DATA VALID (-)
4	COMPOSITE SYNC (+)	23	COMPOSITE SYNC (-)
5	FIELD INDEX (+)	24	FIELD INDEX (-)
6	VIDEO DB9 (+) (LSB FOR DVC-10)	25	VIDEO DB9 (-) (LSB FOR DVC-10)
7	VIDEO DB8 (+)	26	VIDEO DB8 (-)
8	VIDEO DB7 (+) (LSB FOR DVC-08)	27	VIDEO DB7 (-) (LSB FOR DVC-08)
9	VIDEO DB6 (+)	28	VIDEO DB6 (-)
10	VIDEO DB5 (+)	29	VIDEO DB5 (-)
11	VIDEO DB4 (+)	30	VIDEO DB4 (-)
12	VIDEO DB3 (+)	31	VIDEO DB3 (-)
13	VIDEO DB2 (+)	32	VIDEO DB2 (-)
14	VIDEO DB1 (+)	33	VIDEO DB1 (-)
15	VIDEO DB0 (+) MSB	34	VIDEO DB0 (-) MSB
16	GROUND	35	GROUND
17	RESET	36	
18		37	
19			

Table 5-3: "Y" cable: Pinout of Digital DB-37 connector (marked "D")

5.9 Gamma Correction

5.9.1 Definition:

Gamma is a measure of the linearity of the camera's response to light.

The CCD is inherently a linear device. The output signal is directly proportional to the scene llumination (or exposure). Doubling the exposure, will double the output signal.

The phosphors that are used to make monitors are non-linear; typically, the phosphors have less brightness response for dark signals and more brightness response for bright signals. This characteristic is shown in Figure 5-9 as a concave exponential brightness curve in response to a linear camera signal. Most phosphors have a $\gamma > 1$; a typical value is 2.2; see section 5.5.2 for a definition).

To compensate for this, the opposite kind of non-linearity is introduced in the output video of the camera. The Video Processor adds gain for dark signals and reduces the gain for bright signals in such a way that the overall system (camera and monitor) produce a linear effect ! This non-linearity is called Gamma (γ) correction.

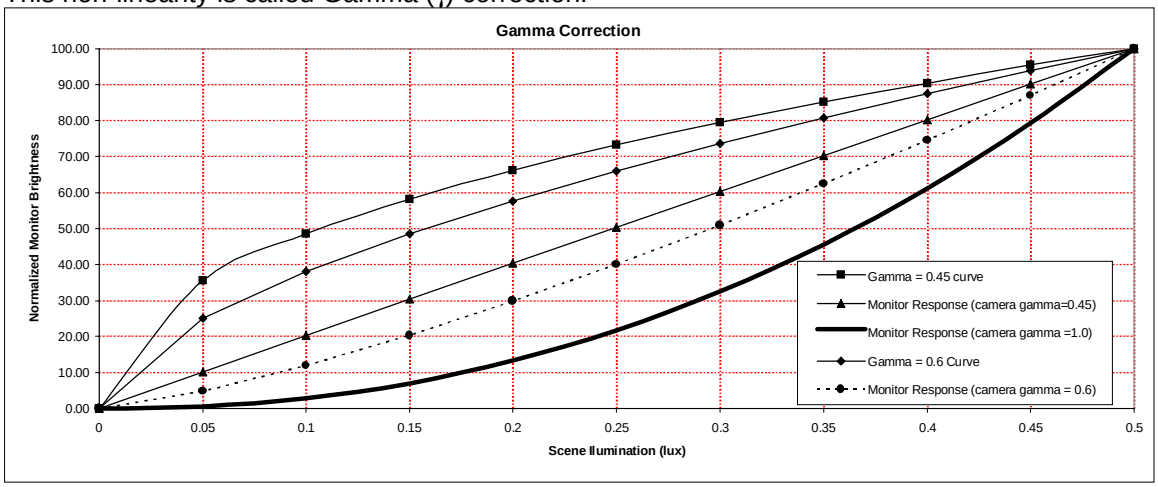

Figure 5-12: Gamma Correction Curves

A gamma setting of 1.0 represents a linear camera response to scene illumination - if the camera is connected to an Image Processor for measurement applications, this is usually desired. However, as seen in the above figure, if the gamma setting of the camera is 1.0 , then the monitor has a non-linear, concave, exponential response to scene illumination. Details in the darker part of an image will not show up with as much contrast as details in the brighter part of an image.

A gamma setting of 0.45 in the camera results in a non-linear, convex, exponential camera response to scene illumination (not appropriate for measurement applications). However, due to the monitor's concave, exponential characteristic this leads to a linear monitor response to scene illumination.

5.9.2 Gamma Equations:

Mathematically, gamma correction is represented in the following manner:

$$\frac{\text{Monitor Brightness 2}}{\text{Monitor Brightness 1}} = M \times \left(\frac{\text{Camera signal 2}}{\text{Camera signal 1}} \right)^{\gamma}$$

M = Monitor Response (brightness/mv of camera signal)

For a typical monitor, $\gamma = 2.2$; hence the concave, exponential curve if a linear camera signal is used. To compensate for this, the opposite kind of non-linearity is introduced in the camera, which modifies the linear characteristic of the CCD as follows:

$$\frac{\text{Camera signal 2}}{\text{Camera signal 1}} = C \times \left(\frac{\text{Exposure 2}}{\text{Exposure 1}} \right)^{\frac{1}{\gamma}}$$

C = Camera Response (mv/lux of scene illumination)

The reciprocal of 2.2 is 0.45; if the gamma correction in the camera is set to 0.45, the overall system response to scene illumination will be linear.

5.9.3 Fixed Gamma Settings in DVC Cameras:

There are three possible settings for Gamma in DVC cameras:

- Gamma = 1.0; This is the default and is ideal for image processing applications ! Most image processing applications use the linear response of the CCD to measure the relative brightness of objects within the field of view. After processing, a Look-up-Table may be used in the Image Processor prior to viewing the processed image on a monitor.
- Gamma = 0.45; This is used when the output of the camera is connected directly to a monitor, without any image processor. This setting leads to an overall system response that is linear. However, due to the increased gain in the dark signal regions of the image, it increases the noise in the image.
- Gamma = 0.6; This is a compromise between a Gamma of 0.45 (with the increased noise) and Gamma = 1.0 (no correction). The curve tracks the Gamma = 0.45 curve at the higher signal levels but does not add as much noise in the lower signal area.

5.9.4 Adjustable Gamma Setting in DVC Cameras:

An adjustable Gamma correction is also available; the user can adjust a Gamma control potentiometer to select Gamma correction from 0.45 to Unity. This is not available on all units; Call DVC for further information !

5.10 ACCESS PORTS :

Upto five access ports are provided on the top surface of the camera cover, as shown in the figure below:

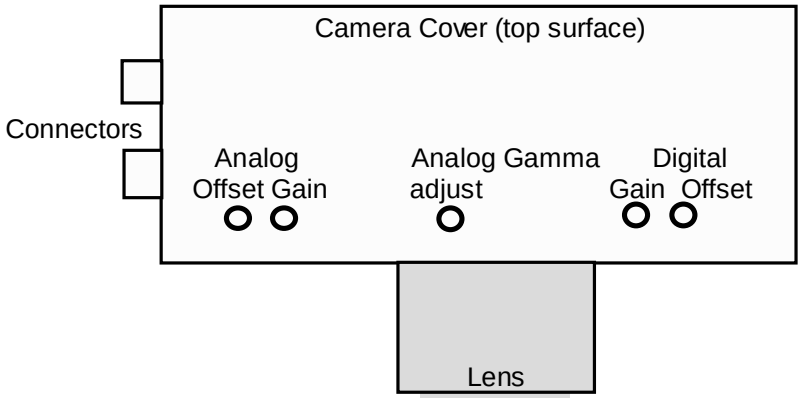

Figure 5-13: Access Ports (Top view)

5.10.1 Access port for analog gain control :

Access to the internal analog gain control potentiometer is provided via a 1/8" hole in the camera cover. The range of operation is approximately 30dB; It has a linear response.

Note (1): The increase of gain increases the noise that is present on the video signal; the signal-to-noise ratio of the analog video signal is considerably degraded in low-light, high gain situations. However, some scientific applications benefit greatly from the External Gain Control function. Since DVC cameras have much higher signal-to-noise ratios than average analog video cameras, they produce much less noise (even in low-light, high gain situations) than most competing products.

Note (2): The analog gain potentiometer is factory set via a special calibration procedure to get the maximum sensitivity without violating the SNR specification of the camera. This potentiometer should only be adjusted in special situations by qualified operators.

5.10.2 Access port for analog offset control:

Access to the internal analog offset control potentiometer is provided via a 1/8" hole in the camera cover. The range of operation is approximately 0-15 IRE; It has a linear response.

Note (1): The RS-170 standard specifies a "setup" or "pedestal" of 7.5 IRE units. This is obtained approximately half-way through the adjustment range - actual settings will vary slightly from unit to unit. The analog offset potentiometer is factory set via a special calibration procedure for 7.5 IRE. This potentiometer should only be adjusted in special situations by qualified operators.

5.10.3 Access port for digital gain control:

Access to the internal digital gain control potentiometer is provided via a 1/8" hole in the camera cover. The range of operation is approximately 10dB; It has a non-linear response.

Note (1): The increase of gain increases the noise that is present on the video signal; the signal-to-noise ratio of the analog video signal (prior to digitization) is considerably degraded in low-light, high gain situations. This can degrade the Effective Number of Bits (ENOBs) of the digital video signal. However, some scientific applications benefit greatly from the External Gain Control function. Since DVC cameras have much higher signal-to-noise ratios than average

analog video cameras, they produce much less noise (even in low-light, high gain situations) than most competing products.

Note (2): The digital gain potentiometer is factory set via a special calibration procedure to get the maximum sensitivity without exceeding the quantization noise threshold of the A/D converter. This potentiometer should only be adjusted in special situations by qualified operators.

5.10.4 Accesss port for digital offset control:

Access to the internal digital offset control potentiometer is provided via a 1/8" hole in the camera cover. The range of operation is +33% and -100% (at the -100% offset point, there is no longer any usable video signal. The Digital Offset control has a linear response.

Note (1): The digital gain potentiometer is factory set to "0" via a special calibration procedure. This potentiometer should only be adjusted in special situations by qualified operators.

5.10.5 Access port for adjustable analog Gamma control :

An internal analog gamma control potentiometer is provided (instead of a standard 0.45 or 1.0 select switch). The range of operation is from 0.45 to 1.0 (Unity gamma). A Gamma value of 0.45 is obtained by adjusting the potentiometer to the one extreme position; unity gamma is obtained by adjusting the potentiometer to the other extreme position. Values between 0.45 and 1.0 are obtained in between the two extreme positions.

6. DVC Camera Image Processor Compatibility

Note: The Analog Video (RS-170) Output of the DVC-0A, DVC-08 and DVC-10 will work with all Image Processors that can accept standard RS-170 Video, including but not limited to, the boards on the following list. (Updated March 10, 1997)

6.1 IBM (PCI)

Manufacturer	Board name / no.	Comments / Status
Matrox	Pulsar Pulsar L/C (without VGA Genesis	Available from DVC
MuTech	MV-1000-10	Available from DVC
Imaging Technolgy Inc.	IC-PCI/AM DIG IM-PCI/AM DIG	Available from DVC
Dipix	XPG-1000 FPG-44 LPG-132	Available from DVC
Active Imaging	Snapper BIB	Available from DVC
Bitflow	Data Raptor Roadrunner (RS-422 only)	Available from DVC
Coreco	F/64 Oculus TCI-Digital Digital-SE RS-422 only	Available from DVC
Precision Digital Imaging	IMAX-PCI	Available from DVC
Epix	PIXCI	RS-170 only (8 bits)
Imagraph	Imascan precision	RS-422 only (8 bits)
Univision	Falcon PCI Falcon XL	

6.2 IBM-PC

Manufacturer	Board name / no.	Comments / Status
Imaging Technology	AFG MFG 150/40	Available from DVC
Matrox	1280 640 L/C Magic	Available from DVC
Dipix	P-360	Available from DVC
Coreco	OC-500 F/64	Available from DVC
Hyperspeed	Hyperspeed	
Alacron		
Ariel		
Cognex	5600	

6.3 MAC (PCI)

Manufacturer	Board name / no.	Comments / Status
Active Imaging	Snapper BIB	Available from DVC
Precision Digital Imaging	SD-Board	Available from DVC
Bitflow	Raptor-VL	Available from DVC

6.4 VME

Manufacturer	Board name / no.	Comments / Status
Imaging Technology	IMA-DIG	Available from DVC
DataCube	MV-200	Available from DVC

6.5 SUN (S-BUS)

Manufacturer	Board name / no.	Comments / Status
EDT	SDV	Available from DVC
Active Imaging	Snapper BIB	Available from DVC

6.6 SGI Digital

Manufacturer	Board name / no.	Comments / Status
SGI	O2	DVC can build a box to match this parallel, digital video interface
SGI	Indy	DVC can build a box to match this parallel, digital video interface
SGI	Indigo2	DVC can build a box to match this serial, digital video interface

7. Ordering Information & Model Index

7.1 DVC "DigitEyes" CAMERA MODEL INDEX

Mfr.	Bits	Synch. options	Elect. Shutter	"N" Field Integ.	Pulse Driven Integ.	Optical Filter	Analog Gain	Analog Offset	Access Ports	Analog Gamma	Index
DVC	XX	S	E	N	D	I	G	O	P	Y	
		None	None	None	None	None	Internal	Internal	None	0.45	**0**
		Genlock	Yes	Yes	Yes	IR Filter	External	External	User sp.	1.0	**1**
		Asynch. reset				User sp.	AGC (30dB)			0.6	**2**

Typical microscopy camera example: To order an analog video camera, external analog gain/offset control (with remote control gain/offset box) and analog gamma of 1.0, order the following:

Table 7-1: DVC-0A Ordering Example

Mfr.	Bits	Synch. options	Elect. Shutter	"N" Field Integ.	Pulse Driven Integ.	Optical Filter	Analog Gain	Analog Offset	Access Ports	Analog Gamma
DVC	XX	S	E	N	D	I	G	O	P	Y
	0A	0	0	0	0	0	1	1	0	1

Example Model no: DVC-0A-0000-01101 with remote gain/offset box.

Typical digital camera example: To order a 10 Bit digital camera with asynchronous reset; pulse driven integration; access ports for analog gain, digital gain & offset; and analog gamma = 1.0, order the following:

Table 7-2: DVC-10 Ordering Example

Mfr.	Bits	Synch. options	Elect. Shutter	"N" Field Integ.	Pulse Driven Integ.	Optical Filter	Analog Gain	Analog Offset	Access Ports	Analog Gamma
DVC	XX	S	E	N	D	I	G	O	P	Y
	10	2	0	0	1	0	0	0	1	1

Example Model no: DVC-10-2001-00011 with 3 access ports: for analog video gain, digital video gain and offset.

8. Frequently Asked Questions (adapted from DVC's WWW site)

8.1 PRODUCT INFORMATION

8.1.1 What is the "DigitEyes" product series?

DigitEyes is a new family of real time monochrome video cameras introduced by DVC Company. The family includes the baseline DVC-0A analog RS-170 video camera, the DVC-08 eight bit digital video camera with simultaneous analog RS-170 output and the DVC-10 ten bit digital video camera with simultaneous analog RS-170 output.

Some features of the DigitEyes family of cameras include:

- Extremely "quiet" performance; in SHARP contrast to "security & surveillance" cameras that produce "snowy" images!
- High sensitivity
- Real time (30 frames/sec) video generation
- Opto-mechanical precision for repeatability in high-end measurement applications; in SHARP contrast to non-scientific grade "security & surveillance" cameras with imprecise optical mounts !
- Elimination of pixel jitter with digital output
- Compatible with Image Processors for a variety of platforms (including IBM-PC, PCI, Mac-Nubus, SGI Digital, VME & S-BUS)
- Rugged construction; suitable for challenging OEM environments. Board level cameras are available.
- Uses industry standard C-mount lenses

8.1.2 What are the differences between the DVC-0A, DVC-08 and DVC-10 products?

- The DVC-0A is the "baseline" RS-170 analog video only camera.
- The DVC-08 is an eight bit digital video camera with simultaneous analog RS-170 output.
- The DVC-10 is a ten bit digital video camera with simultaneous analog RS-170 output.

8.1.3 I've heard your cameras described as "upgradeable". What does that mean to the user?

The DVC-0A, DVC-08 and DVC-10 cameras are identical in appearance and size. The user can purchase a DVC-0A "baseline" RS-170 analog video only camera for a system that is not setup to handle digital video. The DVC-0A can then be sent to the factory for an upgrade to convert it

to a DVC-08 or a DVC-10 for a nominal upgrade fee (in addition to the difference in the list price of the two models). This enables the user to purchase a camera that will "grow" with his system. No other changes in the power supply, optics or system design are required. Of course, a digital interface cable will be required to use the digital video output.

8.1.4 What kind of a warranty is available on DVC products?

A two year warranty is available on all DVC products. See the “Warranty” section of this manual for details !

8.1.5 Are your cameras available in board form for OEM applications?

Yes. All three models (DVC-0A, DVC-08 and DVC-10) are available in board form.
The DVC-0A board set consists of two boards:

The sensor and video board (3" X 4")
The sync and power board (3" X 4")

The DVC-08 and the DVC-10 board sets consist of the above two boards and an Analog-to-Digital board. The DVC-08 board set uses the AD-08 (eight bit) board; the DVC-10 board set uses the AD-10 (ten bit) board. The dimensions of both AD-08 and AD-10 boards are 3" X 1.5"; the dimensions of the combined board set using all three boards (DVC-08 or DVC-10 models) is 3" X 4" X 1.5"

An optical plate is also available with a C-mount lens adaptor for all three board sets.

This is intended for OEM applications in which the camera electronics are inside the OEM's enclosure. The upgrade policy that applies to standard cameras also applies to board level products.

Please call DVC for details about the board level products !

8.2 SYSTEM ISSUES

8.2.1 What is the minimum system configuration I need to use DVC cameras?

To use a DVC camera you need the following:

- C-mount lens (usually not supplied)
- Camera power supply with DIN connector (usually supplied, available in wall mount or table-top versions, both for the 115V, 60 Hz and the 220V, 50 Hz standards)
- Monochrome RS-170 Video monitor
- Co-axial cable (75 Ω) between the camera BNC connector and the monitor or Image Processor.
- Interface cable (optional for DVC-0A, mandatory for DVC-08 and DVC-10)

8.2.2 Should I use a digital or an analog camera?

This is application dependent. If the camera is used as a source of good, clean video that will not be processed in any way (viewed directly on a monitor), a DVC-0A analog-only camera will suffice. If the video output from the camera will be processed (as in a frame grabber / image processor), you have two possible solutions:

1. Use a DVC-0A analog-only camera and feed the output to the Image Processor. With this solution, there is always the possibility that the "super-quiet" video of the DVC-0A gets noise added to it within the Image Processor before it is digitized. This may lead to non-optimum results even with a good, "high-end" image processor. That's due to the fact that the Image Processor typically resides in a computer that is a noisy, digital environment !

2. Use a DVC-08 or DVC-10 camera with direct digital video output and an Image Processor with a digital video input. Such a system is considerably more immune to noise and is likely to deliver better performance.

8.2.3 What are the benefits of using a digital camera?

8.2.3.1 Effective Number of Bits:

In a DVC digital video camera, the signal-to-noise ratio of the video signal that is being digitized is preserved by taking extreme care in the video processing circuits. The digitization of the video to 10 bits (in a DVC-10) ensures that all 10 bits truly represent data. In a conventional analog video system, the video signal from a high signal-to-noise source (such as the DVC-0A) could have noise mixed into it prior to digitization in the Image Processor's typically noisy, digital environment. Even if the Image Processor is well designed, it derives its power from the computer bus which could be a significant source of noise. The benefits of using a high-end camera and a well designed Image Processor board could easily be lost by adding noise from the computer bus or from another peripheral component (disk drives, video cards etc.) that may be plugged into the same bus ! The addition of this noise could very easily degrade the system performance to that of a 6 or 7 bit system. (See ENOBs)

8.2.3.2 Elimination of pixel jitter:

In an analog video system, the pixel clock is derived from the incoming video via a Phase Locked Loop (PLL). By the very nature of the pixel clock recovery process in a PLL, a certain amount of pixel jitter or uncertainty in the clock transitions is generated. This uncertainty is harmless in applications where the video data is used merely to create pictures. In a high-end application however, where the data is used for measurement, the pixel jitter of a conventional analog video system can lead to inaccurate, non-repeatable results. Note: this would happen with all analog video camera systems, including those using the DVC-0A ! (The fault lies with the PLL action on the Image Processor boards).

8.2.3.3 Sub-pixel accuracy:

In some applications, a Sub-pixel interpolation scheme is employed; this involves using a mathematical algorithm to compute numerous pseudo-pixel values between two real pixel values. Needless to say, the more the accuracy and stability in the two "real" pixel values, the better the response of the sub-pixel interpolation algorithm.

8.2.3.4 Spatial coherence:

A line of analog video data is sampled (digitized) at the PLL derived pixel clock rate in a conventional system. The derived pixel clock is not in any way related to the actual pixel data that was originally used to "create" the line of analog video. Although a reasonable sampled version of the line may be re-created, the actual spatial coherence to the CCD charge sites is lost in a conventional system ! A direct correlation and transfer of the gray level information from the pixel element in the sensor, to a precise memory element within the memory array exists in a digital camera based image processor system.

8.2.4 Do I need a frame grabber to use digital cameras?

Yes; the output data from a digital video camera is a data stream of parallel 8 or 10 bit words. Several "handshaking" signals are also provided. A compatible Image Processor can translate the data streams into "frames" of video by means of storing the video data into the appropriate locations of a frame buffer, based on the information encoded in the handshaking signals.

8.2.5 How should I go about selecting a frame grabber for my application?

1. Determine the software/hardware requirements of the application. Try to figure out the actual image processing that will be required. Not all Image Processors are created alike ! Some are better at image capture and display, others offer better number crunching.

2. Choose the "platform" or the processor bus. (Sometimes this can be a decision based on experience or familiarity with one platform over others !)

3. Consult the List of Compatible Image Processors

8.2.6 Do I need to cool the camera?

With a signal-to-noise ratio of >62 dB and an equivalent number of bits = 10 at 25°C running at a real-time rate of 30 frames/sec, most DVC camera applications can achieve high performance without the cost and complexity of external cooling.

Cooling a CCD sensor reduces flow of the dark current electrons; therefore, cooling a CCD can improve its dynamic range. However, under normal conditions, the dark current for the TC-245 CCD is lower than one LSB (for 1/60 sec integration) and is therefore not very significant. In non-standard modes such as long term integration etc., cooling can be useful

There are two ways to cool the CCD in a DVC camera:

- Due to the unique opto-mechanical design of the DVC camera, the CCD is in thermal contact with the front-plate. Cooling to a temperature that is just above the dew point is possible by simply attaching a cooler to the outside front metal plate. Below the dew point, condensation can be a problem ! To eliminate condensation, the camera can be enclosed in a dry chamber.
- In a vacuum dewar down to -35°C or -40°C. Single stage and multi-stage coolers are available.

Please contact DVC for information.

8.3 PRODUCT FEATURES

8.3.1 What is the single, most important reason to buy a DVC camera vs. the "competition"?

That's easy ! With DVC Cameras you get a terrific combination; high signal-to-noise ratio without sacrificing sensitivity or real-time operation. DVC's real time (30 frames/sec) cameras provide >62 dB SNR at a sensitivity of 0.5 lux. Most high-end commercial cameras are much noisier (lower SNRs), at 0.5 lux OR they just cannot match the sensitivity; low-end cameras produce unusable, noisy video at "max" gain if they try to reach a sensitivity of 0.5 lux !

8.3.2 Can you define the term signal-to-noise ratio ?

The term signal-to-noise ratio of a camera is best described by the following:

Let's say that it takes 0.5 lux of light at the CCD of a camera to produce 100 IRE of video (for the purposes of this discussion, 100 IRE is 1.0 Volts of video signal). If you take away the source of light (by capping the lens), you expect to get 0 IRE of signal, right ?

Sorry, but that's true only in an ideal world !

In the real world, you'll get, for a typical competitor's high-end camera, 0.32 IRE (peak) of randomly varying video signal, (called noise) with the lens capped. That's because, a few pesky electrons called dark current electrons flow in the CCD, even without any light. It's analogous to a leaky faucet, no matter how tightly you close the faucet, a few drops always leak through and get collected in the bucket (the CCD charge site). The random variation in the dark current electrons contribute significantly to the noise in the video signal - this shows up as "snow" in the image on a monitor !

The ratio of the 100 IRE signal and the 0.32 IRE noise is the signal-to-noise ratio.

In this example (not a DVC Camera) the SNR is 100 IRE / 0.32 IRE = 316

The SNR is usually expressed in decibels (dB). SNR (in dB) = $20*\log_{10}$(Signal/Noise)

In our example, the SNR (in dB) is $20*\log_{10}$ (316) = 50 dB (approximately)

The above example is typical of a so-called "security and surveillance" camera. Quite frankly, most of them can't even do 50 dB at a 0.5 lux sensitivity ! To be that sensitive, they have to crank up the gain - but that degrades the SNR much, much below 50 dB !

Beware of camera specifications that use terms like SNR and sensitivity without linking them together ! Any camera can claim to have "super sensitivity". The question is that "What signal-to-noise ratio (how "snowy" a picture) do you have to live with to achieve that "super sensitivity".

The converse is also true; a camera can claim to have "low, low noise" - but it may have to be virtually "blind" in terms of sensitivity to achieve that "low SNR" specification. By de-linking the terms SNR and sensitivity, some camera manufacturers can be awfully creative !

Another trick is to use words such as "usable video" as part of the sensitivity specification. It is more scientific to specify sensitivity as the light required for 100 IRE (full video). Since CCDs are

linear, it is obvious that it takes less light to produce 10% video (or 10 IRE). Obviously a lower sensitivity number can be touted by "redefining" sensitivity at 10% or "usable" video.

Note: The next time you read a camera spec, remember that: The SNR should be specified at a particular sensitivity for it to be a meaningful number ! Also specified, should be the video output (in IRE or in volts) that the sensitivity relates to, for example:

"The SNR for a DVC camera is >62 dB @ 0.5 lux for 100 IRE video" !

In a DVC camera, the noise would be typically < 0.1 IRE (peak) for a 0.5 lux sensitivity.

For the DVC Camera, the SNR is 100 IRE / 0.1 IRE = 1000

The SNR (in dB) for a DVC camera is $20*\log_{10}(1000) = 60$ dB (approximately)

The actual SNR for a DVC camera (at a sensitivity of 0.5 lux) has been measured to be >62 dB

8.3.3 How are Signal-to-Noise Ratio (SNR) and sensitivity related?

First, let's define sensitivity. The sensitivity of a camera is defined as the amount of light (in lux or in foot-candles) that must be incident on the CCD surface to produce a 100 IRE video signal (for the purposes of this discussion, 100 IRE is 1.0 Volts of video signal). In a digital video context, 100 IRE is a pixel value of "255" in an 8 bit system or "1023" in a 10 bit system.

Needless to say, a camera that takes less light to produce a 100 IRE signal, is more sensitive than a camera that takes more light to produce a 100 IRE signal. In other words, when it comes to sensitivity, less is better !

If you increase the amount of video gain in a camera, you can increase the sensitivity. By increasing the gain, it takes less light to create a 100 IRE signal - more sensitivity. Since most video monitors saturate beyond 100 IRE, it is the maximum usable signal.

Unfortunately, by increasing the gain for the signal, you also increase the gain for the noise, usually by the same amount. So, you wind up with a 100 IRE (max) video signal with more noise in it - a lower signal-to-noise ratio.

So, by increasing the gain, you increase sensitivity, but decrease the SNR. Since DVC cameras are "quiet" to start with, you can increase the gain considerably, i.e. make the camera considerably more sensitive before the SNR degrades to what others consider their best mode!

At DVC, we call that our gain margin ! In just about every real camera "shoot-out", researchers turn the lights low and crank up every camera's gain ! That's where DVC's performance shows !

8.3.4 How do the DVC cameras compare with the "mega-pixel" cameras ?

Mega-pixel cameras certainly have their own niche applications. For the most part, however, they do not have the real time performance of DVC cameras (30 frames/sec). The few mega-pixel cameras that are real time are prohibitively expensive ! For a fraction of the price differential, the same performance (with a slightly smaller field of view) can be achieved by using a DVC camera and optical magnification.

The biggest drawback (apart from cost) to using mega-pixel cameras that are out there to-day is the non real-time performance (typically 7.5 frames/sec) and their use of electro-mechanical

shutters (with moving parts). Since they typically use CCD "staring" arrays, an electro-mechanical shutter is required between integration periods ! Apart from the somewhat annoying "ticking" sound, there is also a decreased system reliability by introducing a component with moving parts in an otherwise reliable, solid-state design.

8.3.5 Do I need a digital output camera to benefit from the higher signal-to-noise ratio of DVC cameras?

No; the higher signal-to-noise ratio is found on the DVC-0A analog RS-170 only camera. If you hook it up to a monitor, you'll observe the reduced noise or "snow" on the screen. Compare this against any other video camera that has approximately the same sensitivity.

8.3.6 What is the best way to "benchmark" the DVC camera vs. the “competition" in a side-by-side comparison?

To do a true side-by-side test of the DVC camera vs. the "competition", point both cameras at the same scene, with both lenses at the same f-stop number . This ensures that the same amount of light is incident on both CCDs.

To do an accurate comparison, make sure that the AGC circuits in both cameras are disabled. Use a monitor with an A/B switch, so that monitor settings do not corrupt the experiment !

Usually, you'll find that the DVC camera has a brighter picture (more sensitivity) for the same illumination. Note that this is done without compromising the signal-to-noise ratio of the DVC camera. In order to achieve the same sensitivity in the competitor's cameras, the gain would have to be increased significantly - this would lead to a decreased signal-to-noise ratio (more "snow" in the image).

Now, turn the scene illumination down (use Neutral Density or ND filters, if you can; keep in mind that ND filters are calibrated on a logarithmic scale - so a ND 2.0 transmits 1/100th of the incident light, a ND 3.0 transmits 1/1000th of the incident light).

Turn up the video gain on both cameras till you can see an equally bright picture from both cameras with the same amount of ND filters and the same f-stop of the lens.

This is where you will see the DVC camera outperform the competition - compare the amount of "snow" in both images under low-light, high-gain conditions.

8.3.7 What is meant by Equivalent Number of Bits (ENOBs) ?

In the digital video domain, the signal-to-noise ratio, takes on a more serious role !

When the analog video signal and its accompanying noise component are digitized, the noise tends to corrupt the lower significant bits. In an 8 bit system, the noise may show up as a pixel value with an uncertainty. This means that for a uniformly illuminated "flat" field, digitized pixel values might vary from, say, 80 (or Hex 50) to 83 (or Hex 53). With a noisy signal, the same range might apply for the same pixel location, sampled in successive fields.

Note: the lower two significant bits have been lost to noise in this example ! Obviously, if the analog signal has more noise in it, the result will be that more bits will be lost to noise - lower ENOBs !

The Equivalent Number of Bits in our previous example is no longer 8 but 6 !

Even with an ideal 8 bit Analog-to-Digital converter, the noise in the analog system reduces the Equivalent Number of Bits (ENOBs) to 6.

8.3.8 How does the signal-to-noise ratio (in dB) relate to Equivalent Number of Bits (ENOBs)?

A useful formula to convert SNR (in dB) to ENOBs and vice versa is: SNR = 6*N + 2
SNR is the signal-to-noise ratio (in dB) and N is the Equivalent Number Of Bits.

The above formula (SNR = 6*N + 2) can be derived as follows:

The dynamic range (or the "minimum" SNR) of a system with N "true" bits is 2^N.

The dynamic range (in dB) for a system with N "true" bits is $20 * \log_{10}(2^N)$

=> SNR = $N * 20 * \log_{10}10(2) = 6.02N$; Since $20*\log_{10}10(2) = 6.02$

This is approximately equal to 6*N. An additional 2dB are added due to quantization noise in the Analog-to-Digital conversion.

=> the minimum SNR for an N bit system should be = 6*N + 2

If N=6, SNR = 6*6 + 2 = 38 dB
If N=7, SNR = 6*7 + 2 = 44 dB
If N=8, SNR = 6*8 + 2 = 50 dB
If N=9, SNR = 6*9 + 2 = 56 dB
If N=10, SNR = 6*10 + 2 = 62 dB

From the above examples, it can be inferred that in order to have a system that is "true" 8 bits, the SNR of the video signal to be digitized must be > 50 dB. Note: this SNR relates to the signal AT the Analog-to-Digital converter of the Image Processor (not at the output of the camera) !

The average "security and surveillance" analog camera has 50 dB at the camera output.

By the time the video is processed in the front end circuits of the Image Processor in a noisy computer environment, it is likely to pick up a considerable amount of noise. A typical signal at the Analog-to-Digital converter would have 42 dB of SNR ! This would mean that even with an "ideal" Analog-to-digital converter, the system would have only 6 Effective bits !

It is pretty clear that the only way to "preserve" the ENOBs of the system and make it insensitive to noise and to system effects that are outside the control of the designer is to digitize the video within the camera. Once the video data is digitized, the ENOBs will be maintained even in a noisy system.

8.3.9 Why would I need to control the Gain of the Camera in my application?

In some applications, it is important to "tune" the dynamic range of the camera to that of the application.

8.3.9.1 Low Light Applications

If a low-light application requires that a very small amount of light creates a significantly large video output, then an increase of the video gain may be required. Note: the increased video gain will create a more sensitive camera, but the noise in the image will increase !

8.3.9.2 Large intra-scene Dynamic Range

An application may produce plenty of light, but the purpose of the application might be to discern image details in the bright part of an image as well as in the relatively darker parts of the image. A low gain setting will be useful in imaging the entire dynamic range.

8.3.9.3 Automatic Light Control

If an application has to deal automatically with variable light conditions, a camera with the AGC (automatic Gain control) may be suitable. This could be made to work with the Auto-Iris feature to provide an increased range of light variation.

See section 5.4 for More Details on Gain/Offset control

8.3.10 How is the "Back Focus distance" set on DVC's DigitEyes cameras ?

The Back Focus distance is the distance from the back of the lens system to the surface of the CCD. Most "security and surveillance" cameras use inexpensive rubber tipped set screws to hold the C-Mount ring and thus set the back focus distance! While this works well for security and surveillance applications, it is not recommended for high-end image processing applications.

In order to achieve opto-mechanical stability and repeatability, a different approach was taken in the design of the opto-mechanical sub-system of the DigitEyes cameras. The C-Mount ring (into which the C-Mount lens is screwed in) itself screws into an outer ring. A "lock nut" or "compression ring" that screws onto the outer thread of the C-Mount ring is then used to lock down the C-Mount ring.

In order to set the Back Focus distance:
1) Screw in the lens till it is tightly set in the C-Mount ring.

2) With the power supply connected and the output of the camera connected to a monitor, point the lens of the camera at a distant scene; use sufficient ND filters so that the iris of the lens is wide open and the image (on the monitor) is not saturated.

3) Set the focus distance of the lens to infinity (∞).

4) Loosen the lock nut of the DVC camera.

5) Unscrew (or screw in) the lens and the C-Ring together until the image of the distant scene comes into sharp focus.
6) Tighten the lock nut; the Back Focus distance is now set for the lens! Changing the lens may require re-adjusting the Back Focus distance.

8.3.11 How do I access the user adjustable controls?

CAUTION: DUE TO THE PRESENCE OF STATIC SENSITIVE COMPONENTS WITHIN THE UNIT, ALL INTERNAL CAMERA OPERATIONS SHOULD BE PERFORMED ONLY BY TRAINED TECHNICIANS AT AN ESD FREE WORKSTATION ! PLEASE CONSULT THE DVC COMPANY BEFORE PROCEEDING; SOME INTERNAL OPERATIONS MAY VOID THE WARRANTY !

NOTE: DISCONNECT THE CAMERA POWER BEFORE ATTEMPTING THE FOLLOWING STEPS

In order to access the user adjustable controls within the camera:
Remove the camera cover:

8.3.11.1 Removal of Camera Cover:

Use a 1/16" hex socket driver for the following steps:

1) Remove the three #4-40 screws that hold the connector side panel to the back cover. Do NOT remove the #4-40 screw that holds the connector side panel to the optical front plate.

2) Remove the #4-40 screw on the non-connector side panel that holds the non-connector side panel to the optical front plate. Gently slide the back cover and the non-connector side panel off as a single piece.

Note: The following steps are NOT required for normal access to camera adjustments.

8.3.11.2 Removal of Connector Side Panel:

1) Using a 3/16" nut driver, remove the two hex nuts that hold the DB-37 connector to the connector side panel.

2) Using a suitable wrench, remove the hex nut and lock washer holding the BNC connector to the panel.

3) Using a 1/16" hex socket driver, remove the #4-40 screw that holds the connector side panel to the optical front plate.

4) The connector side panel can now be removed; it continues to be attached to the circuit boards via the internal power supply cable.

Note: In order to access the video processor section, the optical front plate (attached to the C-mount lens adapter) needs to be removed from the video board.

8.3.11.3 Removal of the Optical Front Plate:

1) Place the unit with the lens side down on a flat surface.

2) Using a 3/32" hex nut driver, remove the four black socket head cap screws that hold the video board to the optical front plate. Note that after the screws are removed, the video board is held to the optical front plate by the CCD sensor pins and the CCD sensor socket on the video board.

3) Separate the optical front plate (containing the CCD sensor) from the video board gently while keeping the board parallel to the optical front plate. Twisting the board set during this step can bend the CCD pins and will make re-assembly quite difficult ! The CCD chip is mounted within the optical front plate and should not be removed.

4) After the separation is complete, note the position of pin 1 of the CCD and the corresponding pin of the socket on the video board. Pin 1 on the CCD is identified by its longer length relative to the other pins. On the video board, a triangular mark (near the socket) identifies pin 1 of the socket.

Note: Matching pin 1 of the CCD sensor to pin 1 of the socket on the video board is very important during the re-assembly process.

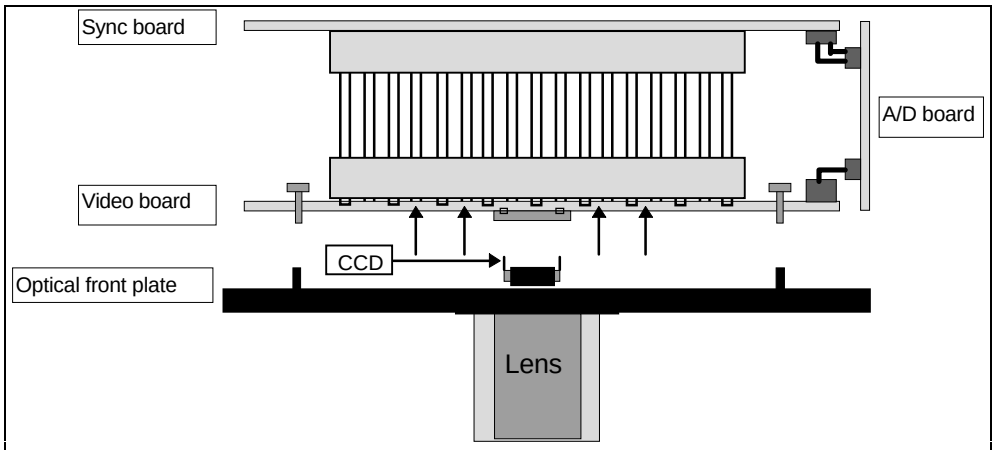

Figure 8-1: Sketch showing Camera boards

Identify the potentiometers and switches in the camera (see next question)

8.3.12 What user adjustable controls are available within the camera?

8.3.12.1 Sync. and Power Board

There are no user adjustable controls on the sync board.

8.3.12.2 Video Board

The video board has the following controls:

- White Balance potentiometers
- Black Balance potentiometers
- Analog gain potentiometer
- Analog offset potentiometer
- Digital gain potentiometer
- Digital offset potentiometer
- Interlace level potentiometer
- Gamma select switch

8.3.12.3 Video Board Adjustments

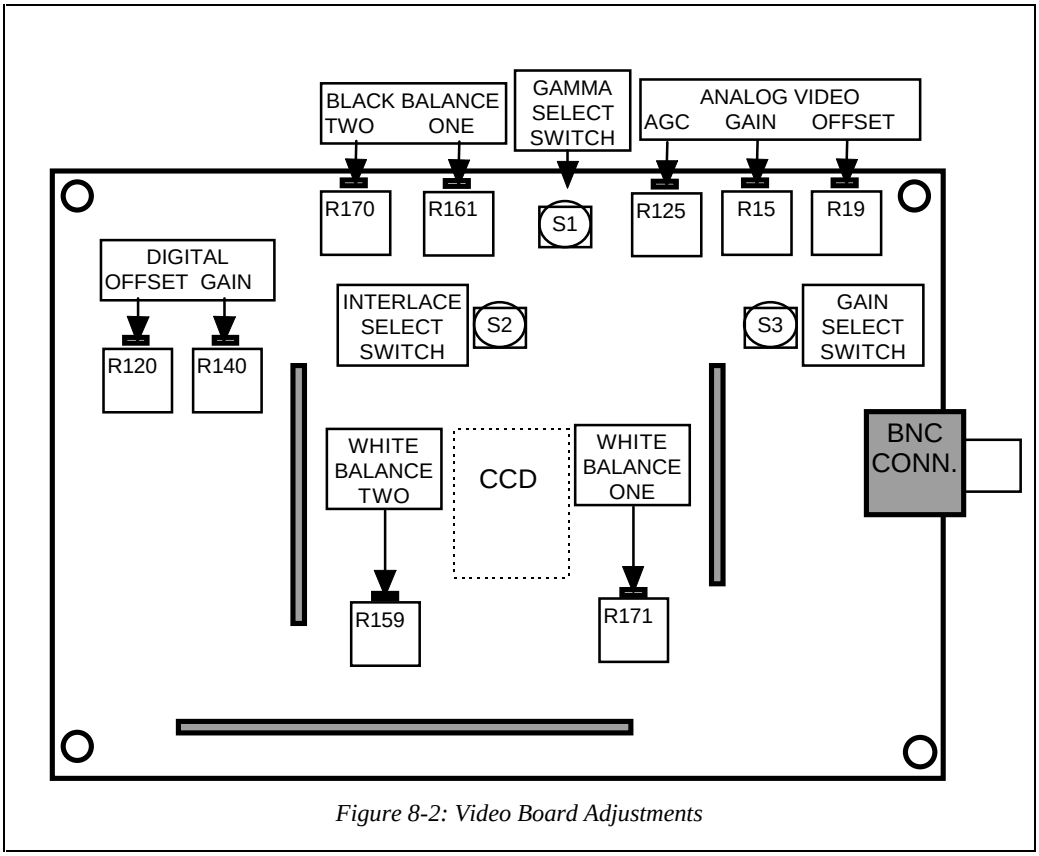

Figure 8-2: Video Board Adjustments

1) BLACK BALANCE ADJUSTMENT: Cap the lens and adjust the Black Balance 1 and Black Balance 2 potentiometers till the vertical fixed pattern noise disappears.

2) WHITE BALANCE ADJUSTMENT: Open the lens and point the camera towards a diffused, uniform field of light (make sure that the camera is not close to saturation). Adjust the White Balance 1 and White Balance 2 potentiometers till the vertical fixed pattern noise disappears.

3) Repeat (1) and (2) in succession till the picture is free from vertical stripes in both situations.

4) GAIN / OFFSET ADJUSTMENT: S3 is a three position switch; the middle position is not used. Setting S3 to the full CCW position selects the AGC mode; setting S3 to the full CW selects the Manual Gain mode. Adjust Analog gain, Digital gain and Digital Offset potentiometers if desired. NOTE: THIS SHOULD NOT BE ATTEMPTED WITHOUT USING A CALIBRATED LIGHT SOURCE AND CALIBRATED OPTICS !

5) INTERLACE ADJUSTMENT: Focus the camera on a suitable target (containing diagonal lines) with approximately 50% video output. Setting S2 (a three position switch) to the full CCW position will create a non-interlaced image (diagonal lines appear jagged, vertical resolution is halved). Setting S2 to the full CW position will create an interlaced image (diagonal lines appear straight, full vertical resolution is obtained). The middle position of S2 is not used.

6) **GAMMA SETTING:** S1 is a three position switch; the middle position is not used. Setting S1 to the full CCW position sets Gamma = 0.45; setting S1 to the full CW position sets Gamma = 1.0

8.4 CCD RELATED QUESTIONS

8.4.1 What CCD sensor is used in the “DigitEyes” cameras? Who manufactures it ?

All the “DigitEyes” cameras use the TC-245 Frame Transfer CCD Imager from Texas Instruments.

8.4.2 What other kinds of CCD sensors are out there ?

In addition to the Frame Transfer CCDs, there are Interline Transfer CCDs and CIDs (Charge Injection Devices). The CIDs have relatively few applications; a comparison of Interline CCDs and Frame Transfer CCDs follows:

8.4.3 How do Frame Transfer CCDs compare with Interline Transfer CCDs?

8.4.3.1 Fill Factor:

Interline transfer CCDs have gaps between the pixels due to their transfer mechanism. This leads to lower fill factors and can present several problems in scientific measurement applications. Frame transfer CCDs have contiguous pixels and a 100% fill factor. This is the reason behind the higher sensitivity of the Frame Transfer CCDs.

8.4.3.2 Size of pixels:

Interline transfer CCDs with the same optical format (1/2") and same number of pixels as comparable Frame Transfer CCDs have smaller pixels (due to the inter-pixel dead space). This makes Interline Transfer CCDs less sensitive than their frame transfer counterparts. The smaller optical format CCDs (1/3", and more recently, 1/4" formats) have even smaller pixel sizes and consequently lower sensitivities. The smaller formats are cheaper to produce, and are quite usable for security and surveillance cameras but are not suitable for scientific work.

8.4.3.3 Full Well capacity:

The smaller size of the Interline transfer CCD leads to a smaller full well capacity. Since the noise floor is approximately the same, the decreased full well capacity leads to a lower Dynamic Range (this translates to a lower signal-to-noise ratio in Interline CCD cameras.

8.4.3.4 Ultra-violet & Infra-red response:

To compensate for the decreased fill factor and smaller pixel sizes, plastic micro lenslet arrays are built on top of the Interline transfer CCD surface to collect the light that would otherwise have fallen on the "dead" inter-pixel gaps. Plastic does not offer good performance down in the UV range below 400nm, and has other limitations at the near IR range. Frame transfer CCDs such as the TC-245 used in DVC cameras, have spectral range of 400-1100nm with CCD glass face plate attached. Customers doing UV work have reported response in the low 200nm range with face plate removed; IR response up to 1100nm has been reported.

Please contact DVC regarding the removal of the CCD glass faceplate for UV response down to the 200nm range ! Do NOT attempt to remove the faceplate, this WILL void the warranty on the CCD sensor.

8.4.4 What is meant by the dynamic range of a CCD ?

The dynamic range of a CCD (or of any measuring system) is a measure of it's range of useful operation. For a CCD this relates to light.

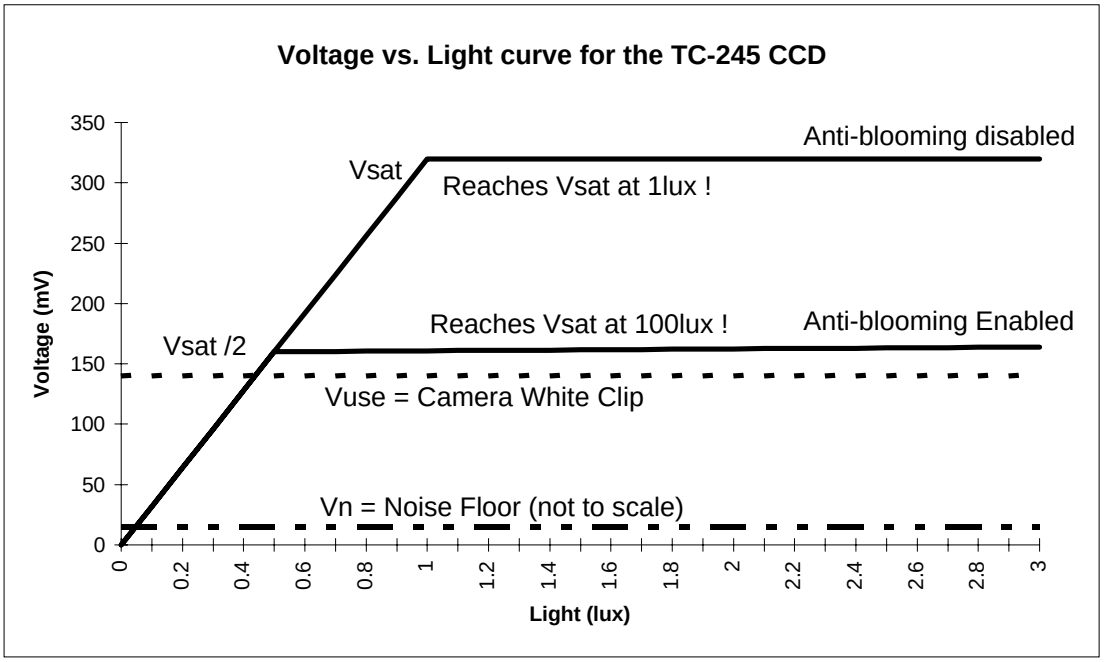

Figure 8-3: Exposure Curve showing the Dynamic Range of the Camera

In the case of the DVC camera, the maximum light that can be measured is 0.5 lux. That's because if more light (than 0.5 lux) is incident on the CCD, the camera will reach 100 IRE (or, in 8 bit digital terms the pixel level of "255").

This operating point is indicated on the above graph as Vuse - the CCD output voltage which will result in 100 IRE units at the output. This is a camera design parameter; Vuse can be moved up the saturation curve by decreasing the camera gain and can be moved down the saturation curve by increasing the camera gain.

Vn (the noise floor, typically 0.08 to 0.12 mV) is a fixed parameter (for a given temperature). The ratio of Vuse / Vn (and therefore the dynamic range) is completely dependent on our choice of Vuse; what this means is that we can "trade off" the camera gain (and hence sensitivity) for the camera dynamic range (hence signal-to-noise ratio).

The other parameter that is important in defining the dynamic range of a camera is the smallest signal that can be accurately measured by it. The physical parameter that limits the smallest discernible signal is the dark current noise.

In a TC-245 CCD sensor, the dark current noise (at 25°C) is represented by the 30 electrons that accumulate at a charge site (often called charge "well") in a normal 1/60 sec integration period if no light is incident on it (this is the worst case, a more typical number is 20 electrons). These electrons are often referred to as "noise equivalent electrons" and constitute a noise floor.

The "full well" figure for the TC-245 CCD (number of light derived electrons required to fill up the charge "well") is 80,000.

The dynamic range of the CCD, therefore, is 80,000 / 30 = 2667
OR expressed in dB, the dynamic range of the CCD is $20*\log_{10}(2667) = 68.5$ dB
The dynamic range (using the more typical 20 noise equivalent electrons) = 72 dB:

A typical CCD dynamic range of 70 dB is assumed. Not all 70 dB of dynamic range is used within the camera; Anti-blooming uses up 6 dB by setting a "knee" at Vsat/2. By setting the Vuse OR “white clip" point slightly below Vsat/2, a dynamic range close to 62 dB is obtained which corresponds well with the >62 dB signal-to-noise ratio of the camera.

8.4.5 What is the image format of the CCD ?

755 (Horizontal) X 484 (Vertical)

The actual number of pixels (charge collection sites) on the CCD are 755(H) X 242(V); the process of pseudo-interlacing creates an effective matrix of 755(H) X 484(V).

8.4.6 What is meant by pseudo-interlaced operation ?

The effective vertical resolution of the CCD is doubled by means of a process called "pseudo-interlacing".

In this process, the charge collection area represented by each pixel is electronically shifted vertically from field to field by half of the pixel height. This is analogous to the process of "dithering" the pixel matrix vertically at 60 Hz. The mechanism of this "dithering" operation and more details (including a diagram) are available below.

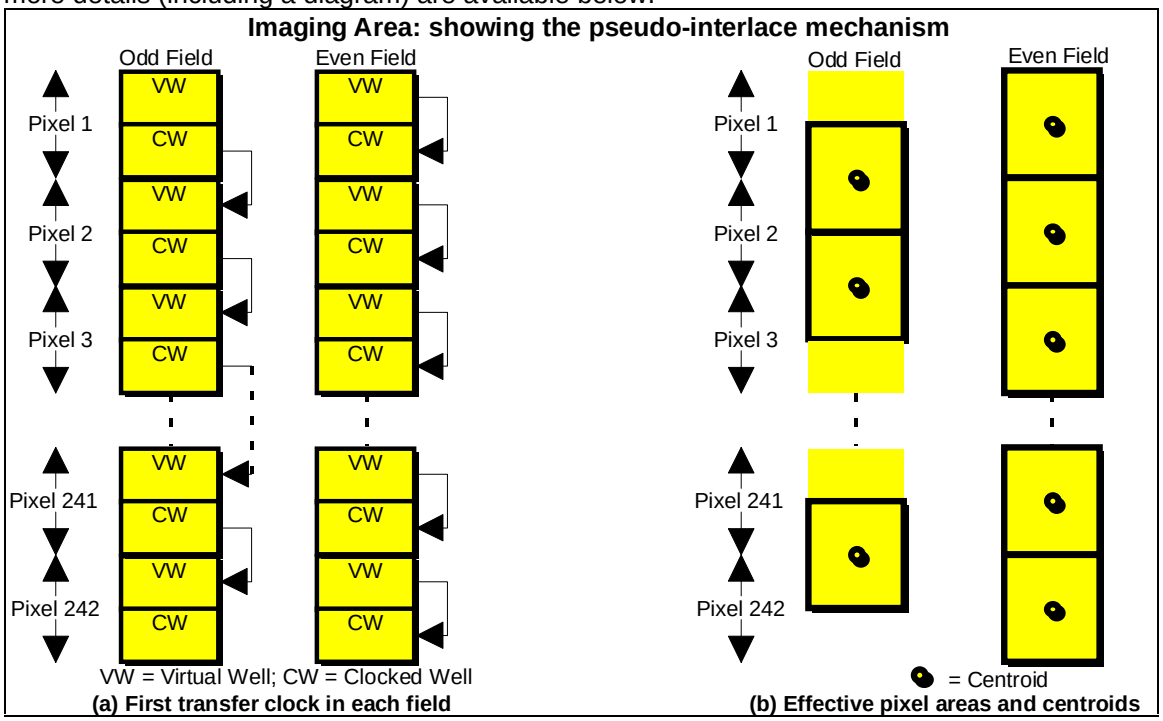

Figure 8-4: Imaging Area, showing Pseudo-interlaced operation

In Figure 8-4, each pixel is shown to have two halves - a Clocked Well (CW) and a Virtual Well (VW). The transfer of charge (that takes place in the vertical blanking interval) uses a slightly different mechanism for the two fields. In the odd field, the first transfer pulse clocks the charge from each CW to the adjacent (lower) VW. In the even field, the first transfer pulse clocks the charge from each VW to the adjacent (lower) CW. As shown in the diagram, this causes the effective pixel area and centroid of each pixel to be shifted by half of the pixel height from the odd field to the even field.

By the above process, the charge collection area represented by each pixel is electronically shifted vertically from field to field by half of the pixel height. This is analogous to the process of "dithering" the pixel matrix vertically at 60 Hz.

Using the two displaced imaging areas, two distinct video fields are created. The resulting interlaced video image may be viewed on a monitor as an image with a higher vertical resolution.

In Image Processing applications, the frame storage memory must be designed in a way that allows the writing of odd-numbered rows during the ODD field and the even-numbered rows during the EVEN field. The FIELD INDEX signal (HIGH during the EVEN field) is provided to simplify the addressing of the frame storage memory.

8.4.7 Can the pseudo-interlaced operation be disabled ?

In applications where a vertical resolution of 242 is sufficient, the interlace operation can be disabled. With the interlace disabled, both fields represent the same physical pixel matrix; the charges, however, are derived from integration periods that are 1/60th of a second (one field period or 16.66 mS) apart.

To disable interlace, the integration level potentiometer on the video board should be adjusted. On more recent versions of the video board, a switch is provided for this purpose.

Contact DVC before making such an adjustment !

8.4.8 What is anti-blooming ?

Blooming: is defined as the phenomenon in which a bright spot of light in the field of view of a video camera appears to be larger in size. Needless to say, this is an unwanted artifact in the image.

Anti-blooming: is the method by which the effect of blooming is minimized (or eliminated).

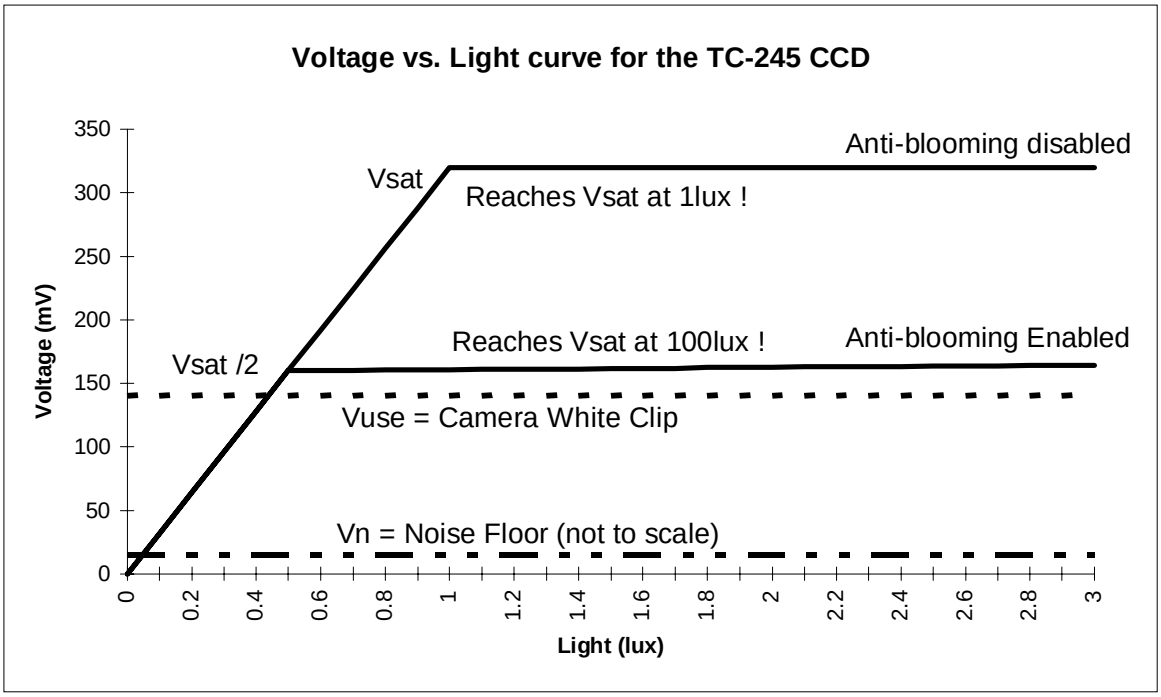

Figure 8-5: Anti-blooming curve

To understand anti-blooming it is convenient to think of a CCD charge site as a mechanism for converting light (photons) to charge (which is then converted to voltage) in a linear manner. The more photons that are incident on a charge site during the integration time (1/60 sec) the more the charge that gets collected in the CCD site; this translates to more voltage corresponding to a particular charge site. The Voltage vs. Light curve is, therefore, linear, with a positive slope.

Unfortunately, there is a limit to the amount of charge that can accumulate in the charge site. Once that limit is reached the charge site saturates and tends to overflow to the neighboring charge sites.

Blooming occurs when a CCD charge site that is exposed to very bright light fills up with charge and then overflows to its neighboring charge sites. The overflow of charge causes a bright spot of light in the field of view of a video camera to appear larger in size. Since the charge sites are like "buckets" full of charge, they can only hold so much charge. When that limit is reached, the charge site is saturated and can hold no more charge.

Continuing with the "buckets" analogy, if the rate at which a "bucket" is filled with water is decreased significantly after it is half-full, then it takes a lot more water to fill it !

If several holes are made in the side of a bucket half way up, the rate at which the bucket is filled decreases significantly once it is half-full.

For a CCD charge site, this is achieved by decreasing the positive slope in the Voltage vs. Light curve. This can be described as a deliberately introduced "knee" in the Voltage vs. Light curve beyond which the slope of the curve is significantly reduced. Although the slope is still positive, it takes a lot more light to reach the saturation point.

The slope of the curve is reduced by means of electron-hole recombination via the anti-blooming gate which is built into each CCD charge site. The excess charge is dumped into the substrate of the device.

In the TC-245 CCD with the anti-blooming function is turned on, the CCD can withstand 100 times the amount of light that would have produced saturation without the anti-blooming function. As shown in the above figure, the CCD would saturate at 1 lux with Anti-blooming disabled but would saturate at 100 lux with Anti-blooming enabled.

The effectiveness of the anti-blooming function is defined as the blooming overload ratio.

This is calculated as the following:

$$\text{Blooming Overload Ratio} = \frac{\text{Light (in lux) reqd. to saturate the CCD with Antiblooming ON}}{\text{Light (in lux) reqd. to saturate the CCD with Antiblooming OFF}}$$

For the above example (see figure above) the Blooming overload Ratio = 100

8.4.9 Can anti-blooming be disabled ?

Yes; the anti-blooming function can be disabled. In some applications, where the light level is carefully controlled and a larger linear region of operation is required, it is possible to disable anti-blooming.

If anti-blooming is disabled, any bright spots in the field of view will cause blooming ! Although this does not damage the CCD, it makes the camera difficult to use in most applications.

Note: this is NOT a user adjustment in the camera. Please call DVC to request more information on this modification.

8.4.10 What is meant by integration time ?

Integration time is defined as the duration that charge is allowed to accumulate in the charge sites of the CCD.

8.4.11 What is the integration time in the standard mode of operation ?

The standard mode of operation results in an integration period of 1/60 seconds or 16.66 ms. This is accomplished by means of a transfer of charge from the Imaging Area (sensitive to light) to the Storage Area (opaque to light) every 1/60 sec - the process called Frame Transfer. Both the Imaging Area and the Storage Areas are identical in size (755H X 242V). By transferring the charge matrix once per field (1/60 sec) and by the process of electronically displacing the integration area every field (pseudo-interlacing), a full frame of 755H X 484V is obtained.

Non-standard integration periods can be obtained under certain special modes. These are user selectable by means of logic levels on the Mode select (default High) pins of the DB-37 connector.

Longer exposures are permitted in the integration mode; shorter exposures are permitted in the integration mode as well as in the shutter modes.

8.5 OPTIONS

8.5.1 What non-standard modes of integration are available ?

The three non-standard modes of integration are:

- Electronic Shuttering (1/1000 sec and 1/2000 sec)
- Pulse driven Integration Mode
- “N” field Integration Mode (user specified value of “N”)

8.5.2 What is the difference between electronic shuttering and pulse driven integration ?

Electronic Shuttering is used for integration periods less than 1/1000 sec. The integration takes lace within the vertical blanking interval and the sync and timing of the camera are un-disturbed.

The Pulse driven Integration Mode is used for integration periods greater than 1/1000 sec. Since his is greater than the vertical blanking period, the video timing is usually disturbed.

8.5.3 Do I need a frame grabber for non-standard integration modes ?

For the Electronic Shuttering mode, the image raster on a monitor is quite stable. A frame grabber may be used but is not mandatory.

For the Pulse driven Integration Mode, a frame grabber is usually mandatory.

8.5.4 What is the image format (size) during electronic shuttering and pulse driven integration ?

Since only one field results from each integration on the CCD, the image format is 755(H) X 242(V)

8.5.5 Can I use genlock/asynchronous reset & electronic shuttering simultaneously ?

Yes ! Both Genlock & the asynchronous reset mode work well with electronic shuttering.

8.5.6 What is genlock and how does it work ?

Genlock is an option that is available on all models. When it is installed, a camera can be "locked" to an external source of sync or video.

See section 5.3.3 for more details.

8.5.7 What is auto-iris and how does it work ?

The auto-iris option consists of a servo loop that is made up of the analog video processor and an auto-iris lens. Circuitry within the auto-iris lens examines the video signal from the video processor and compares its amplitude to a preset amplitude. If the video amplitude from the processor is less than the preset level, the iris of the lens is opened wider; if it is more than the preset, the iris is closed down.

This feedback action keeps the level of the video at the preset value over a range of scene illumination. Once the auto-iris lens is wide open, decreasing the scene illumination has no further effect on the auto-iris lens. Typically, the AGC Circuit takes over at this point ! The two circuits work in tandem to increase the effective dynamic range of the camera.

8.5.8 What is GAMMA - it sounds like Greek to me ?

See section 5.9 for details.

8.5.9 What options are available to control the Digital Video gain and offset ?

At present these adjustments are implemented as potentiometers on the video board. They cannot be "remoted" in the way that the Analog potentiometers can. User access to these controls through holes in the camera cover can be provided as a special modification. Contact DVC for details.

9. Appendix A: Camera Connector Information

9.1 Pin Assignments for the DB-37 Digital Video Connector

Table 9-1: Pin Assignments for the DB-37 (female) Digital Video Connector

PIN	SIGNAL NAME	PIN	SIGNAL NAME
1	PIXEL CLOCK (+)	20	PIXEL CLOCK (-)
2	LINE DATA VALID (+)	21	LINE DATA VALID (-)
3	FRAME DATA VALID (+)	22	FRAME DATA VALID (-)
4	COMPOSITE SYNC (+)	23	COMPOSITE SYNC (-)
5	FIELD INDEX (+)	24	FIELD INDEX (-)
6	VIDEO DB9 (+) (LSB FOR DVC-10)	25	VIDEO DB9 (-) (LSB FOR DVC-10)
7	VIDEO DB8 (+)	26	VIDEO DB8 (-)
8	VIDEO DB7 (+) (LSB FOR DVC-08)	27	VIDEO DB7 (-) (LSB FOR DVC-08)
9	VIDEO DB6 (+)	28	VIDEO DB6 (-)
10	VIDEO DB5 (+)	29	VIDEO DB5 (-)
11	VIDEO DB4 (+)	30	VIDEO DB4 (-)
12	VIDEO DB3 (+)	31	VIDEO DB3 (-)
13	VIDEO DB2 (+)	32	VIDEO DB2 (-)
14	VIDEO DB1 (+)	33	VIDEO DB1 (-)
15	VIDEO DB0 (+) MSB	34	VIDEO DB0 (-) MSB
16	GROUND	35	GROUND
17	RESET	36	+5VOLT AUX. POWER OUT
18	MODE CONTROL 0 (Or Offset Control)	37	MODE CONTROL 1 (Or Gain Control)
19	MODE CONTROL 2		

9.2 Pin assignments for the Power Supply Connector

Table 9-2: Power Supply Connector (5 pin DIN)

PIN	SIGNAL NAME
1	GND
2	NC
3	+ 5 VOLTS
4	- 12 VOLTS
5	+12 VOLTS

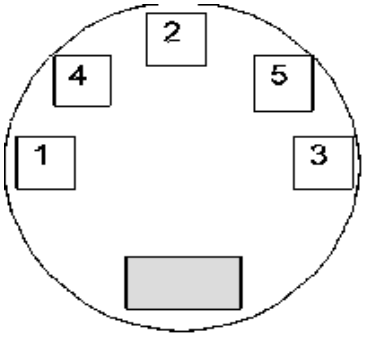

Figure 9-1: Power Supply Connector Pinout Diagram

9.3 Connector part numbers

Table 9-3: Connector part numbers

		Mating Part Information		
Connector	**Mfr.**	**Part No.**	**Mfr.**	**Part No.**
DB37(F) Digital Video Connector	AMP	747847-4	AMP	747916-2
5 Pin DIN Power Supply Receptacle	Switchcraft	57GB5F	Switchcraft	05GM5M

10. Appendix B: Camera Timing Diagram

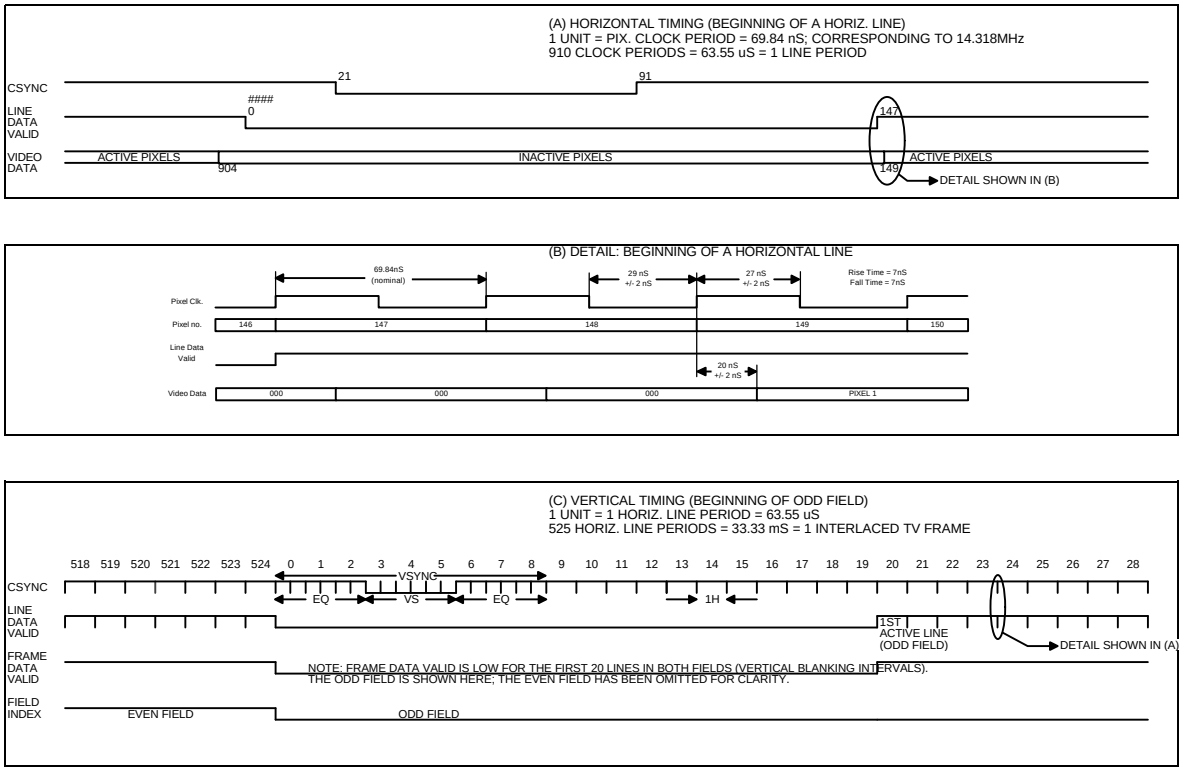

Figure 10-1: Camera Timing Diagram

11. Appendix C: Camera schematic diagram

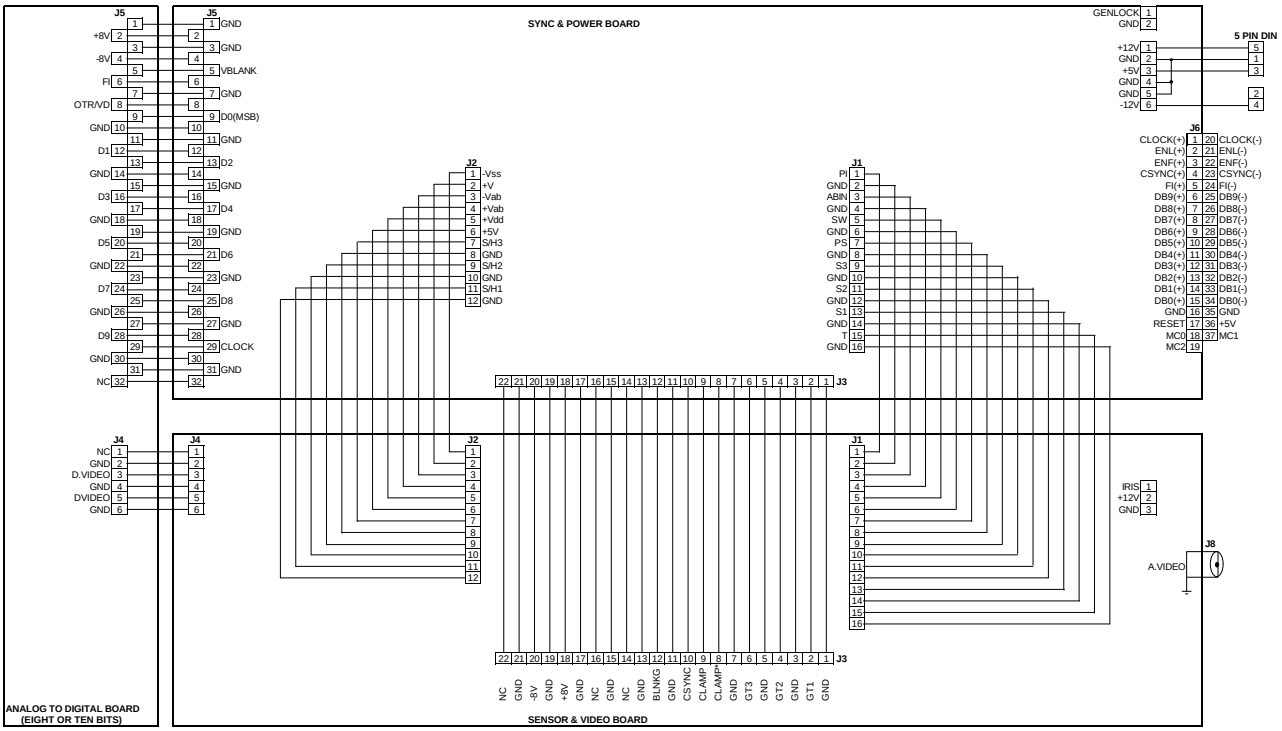

Figure 11-1: Camera Schematic Diagram

12. Appendix D: Camera Mechanical Drawings

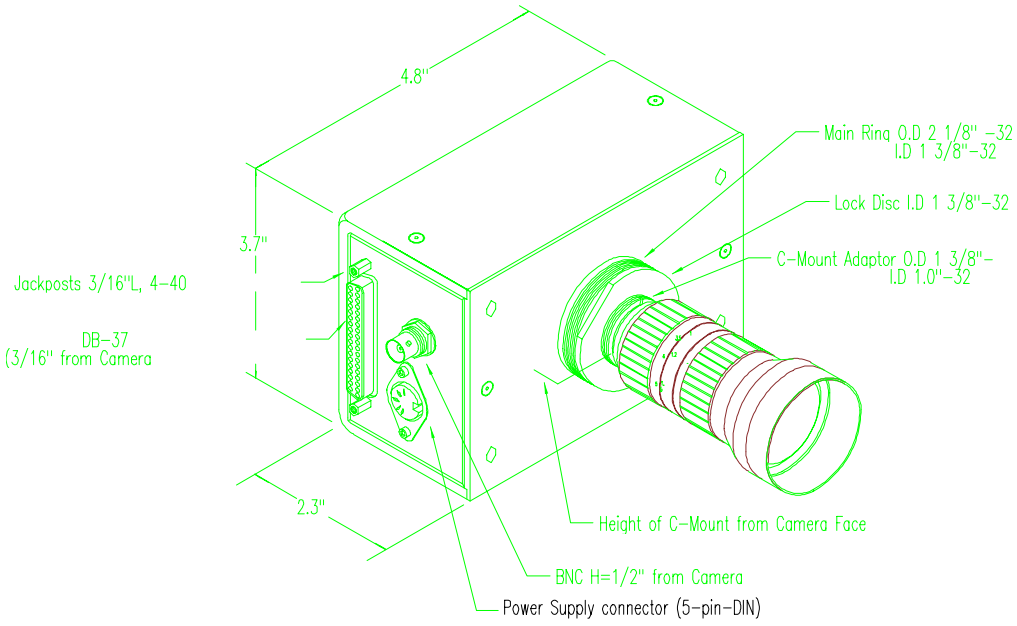

Figure 12-1: Camera Mechanical Drawings

13. Appendix E: Camera Performance Data (VM-700A plots)

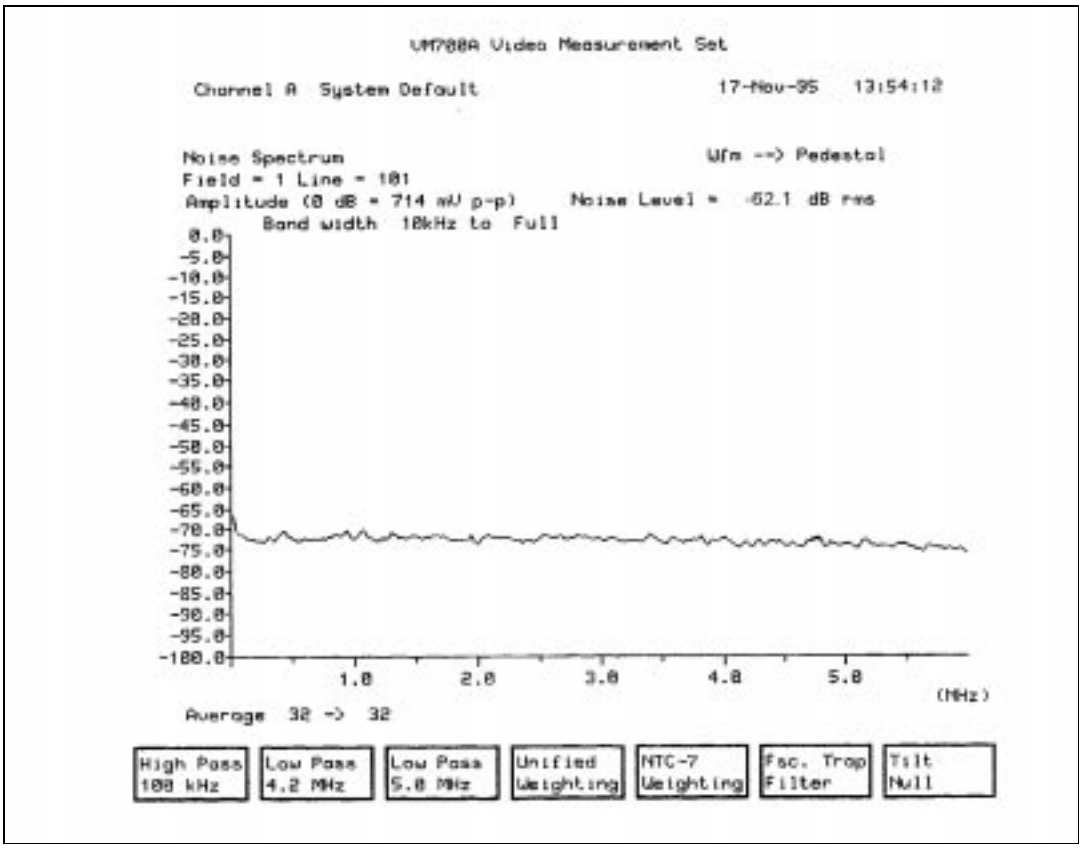

Figure 13-1: Camera Noise Spectrum (Min. Gain, Bandwidth = 10kHz to full)

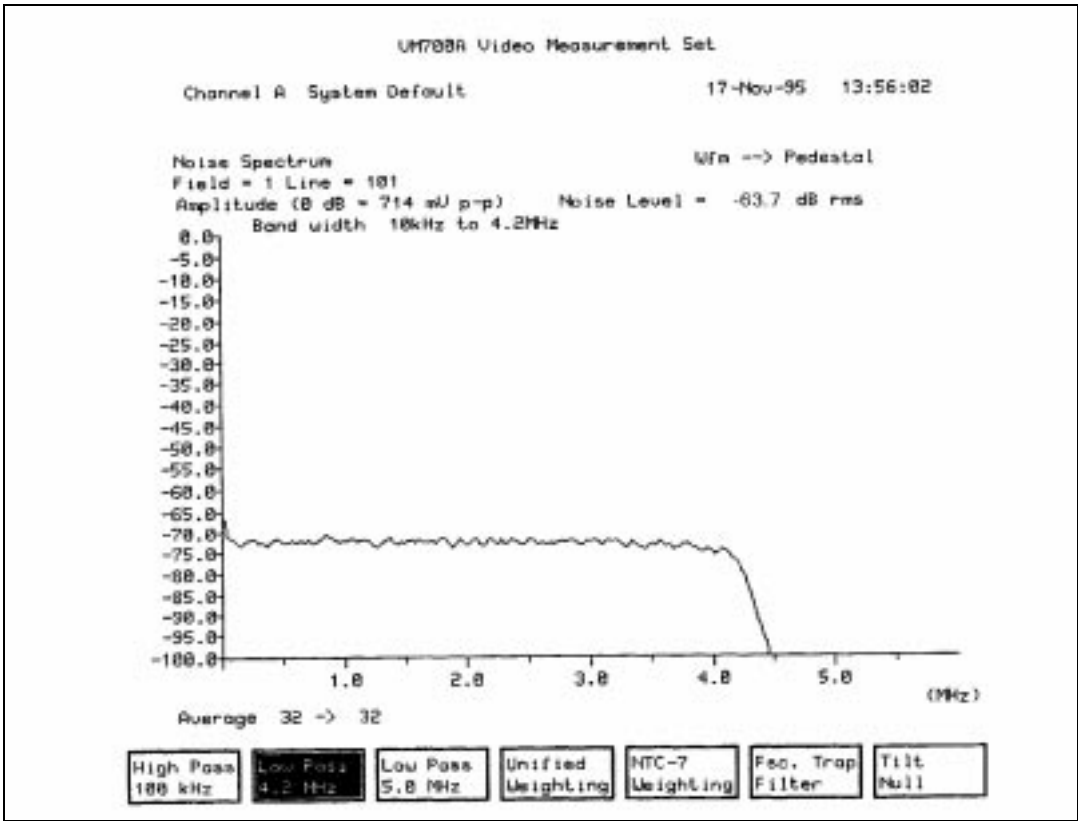

Figure 13-2: Camera Noise Spectrum (Min. Gain, Bandwidth = 10kHz to 4.2MHz)

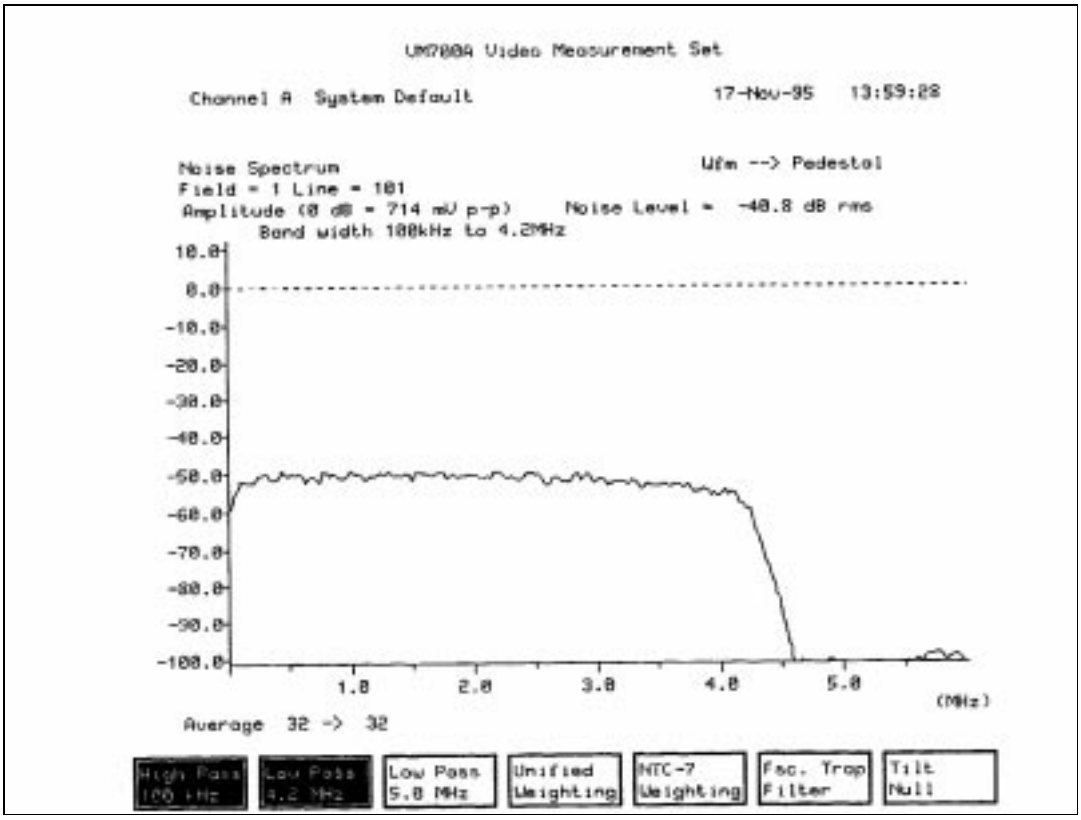

Figure 13-3: Camera Noise Spectrum (Max. Gain, Bandwidth = 100kHz to 4.2Mhz)

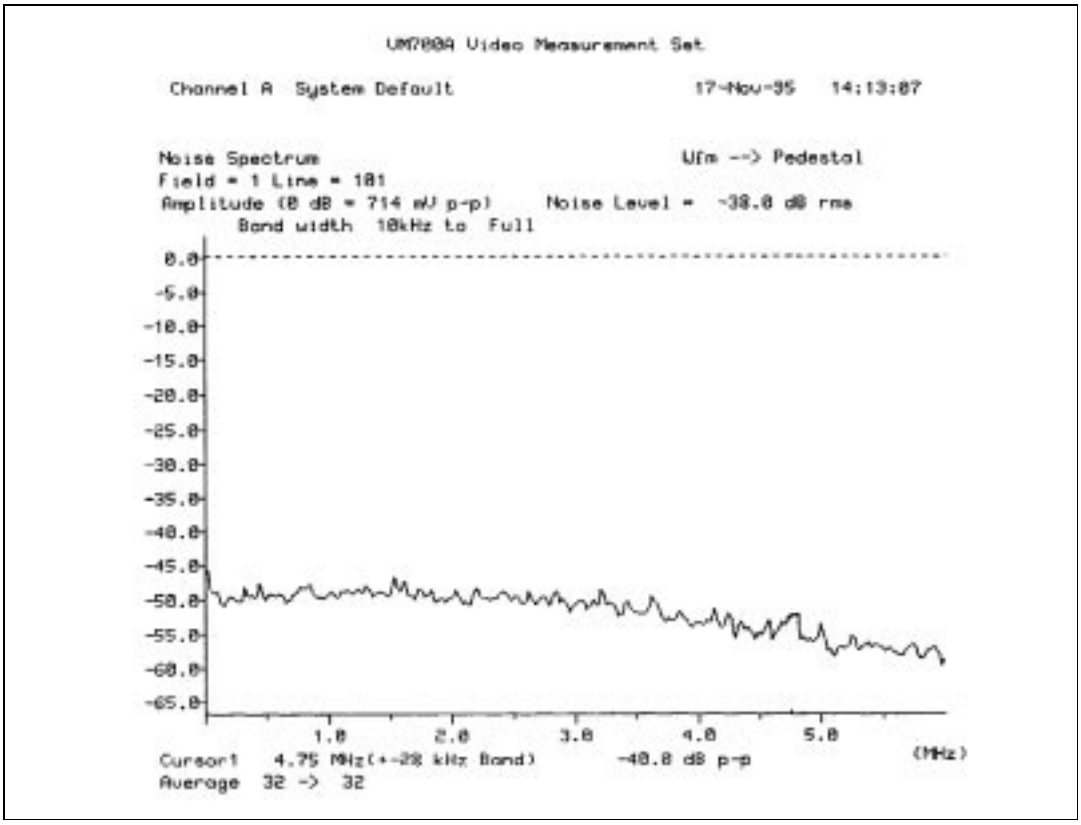

Figure 13-4: Camera Noise Spectrum (Max. Gain, Bandwidth = 10kHz to full)

14. Warranty:

DVC Company warrants equipment manufactured to be free from defects of material and workmanship. Any part or parts will be repaired or replaced when proven by DVC examination to have been defective within two years from the date of shipment to the original purchaser. Any warranty repairs will be performed at the factory or as otherwise authorized by DVC, in writing. Transportation charges to DVC shall be pre-paid by purchaser.

This warranty does not extend to DVC manufactured equipment subjected to misuse, accident, neglect or improper application. Nor does the warranty extend to DVC manufactured equipment that is repaired or altered by anyone other than DVC or those authorized by DVC, in writing. Products manufactured by other companies, but re-sold by DVC such as lenses, optical and electro-optical assemblies, power supplies, cables, image processor boards and software are warranted by the original manufacturer.

This warranty is in lieu of all other warranties expressed or implied. DVC shall not be liable for any collateral or consequential damages.

A Return Material Authorization (RMA) Number must be obtained from DVC prior to returning any item for warranty repair or replacement.

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