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CLinkCam

High-Dynamic-Range Digital Camera with CameraLink Interface

USER MANUAL

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1 INTRODUCTION

CLinkCam is a high-dynamic-range digital camera with CameraLink connectivity, specifically designed for automotive and outdoor applications. Because of its high dynamic range, the camera can be employed over a wide range of lighting conditions without the need of iris adjustments.

CLinkCam's sensor is a monochromatic CMOS sensor of size 640x480 pixels. Each pixel has a 10-bit depth, i.e. the photosensor's signal is quantized into 1024 levels. The response of the pixel is a logarithmic function of the light intensity. The frame rate is 24 full frames per second. Since pixels can be addressed randomly any subset of the 640x480 pixel frame can be captured without the need to acquire the full frame. For this reason, the acquisition speed for selected regions of interest can be greatly increased.

A Xilinx FPGA controls the transfer of data from and to the sensor. The FPGA is programmed to acquire blocks of pixel and to perform fixed-pattern-noise subtraction at frame rate. It also manages three optoisolated I/O lines for synchronized image acquisition and control of industrial devices

2 MAIN FEATURES

- High resolution: 640x480 pixels
- High dynamic range (120 db)
- Logarithmic response to light intensity
- 10-bit pixel depth
- Continuous pixel read-out
- True Random pixel addressing
- 8MHz pixel rate
- Square pixel
- Digital set up
- CameraLink connection
- Three optoisolated I/O lines (one input and two outputs).

3 THE PUPILLA SENSOR

The sensor mounted on CLinkCam is Pupilla, a monochromatic CMOS sensor of size 640x480 pixels. The sensor, realized with active-pixel technology, has a high dynamic range and it is free from blooming.

The six-decades (or 120 dB) dynamic range of the Pupilla sensor is especially useful for the analysis of scenes in outdoor environments where light intensity in a single frame can vary over a wide range. The high dynamic range is a consequence of the logarithmic response of the pixel to light intensity, i.e. $P(I) = A * log (I) + B$, where P is the pixel response, I is the light intensity, and A and B are constant characteristic of each pixel. The logarithmic response is generated by the pixel photocurrent fed into a transistor operating in the weak inversion region. The resulting signal is quantized into 1024 levels by a 10-bit ADC. This means that each pixel is described by a 10-bit word. The logarithmic response implies that

relative variations of light intensity, i.e. $\Delta I / I$, are perceived with constant sensitivity over the whole range. In other words, small changes at low intensity are equivalent to large changes at high intensity.

Continuous readout means that a pixel's photodiode continuously converts the incoming light into a voltage. No charge integration occurs in the sensor and therefore pixels can be read instantaneously (the readout time for a pixel is 135 nsec) at any time. A continuous readout implies that moving objects are not blurred – as in integrating sensors – but only geometrically transformed. The type of transformation depends on the type of motion and in readout order of the pixels. For example, the progressive scan of an object moving at constant speed along the scanning direction, would generate a skew transformation. The skew between successive rows would be 640x135 nsec x Speed pixels/nsec, because successive pixels are read 135 nsec apart.

Because of the active pixel technology, pixels can be randomly addressed: any subset of the 640x480 pixels can be captured without the need to capture the full frame as in a standard CCD. This means that the number of frames per second can be greatly increased if only a part (a Region Of Interest) of the image is needed. Since the pixel rate is 8MHz, the full frame rate is 24 frames per second. The frame rate increases proportionally to the inverse of the ROI area. For example, the frame rate of a subsampled (4:1) image of size 320x240 would be 24*4=96 f/s. The frame rate for a single line acquisition is 480x24=11520 f/s. This characteristic increases the flexibility of the camera and allows the sensor to be used for line scan or high speed, low-resolution applications.

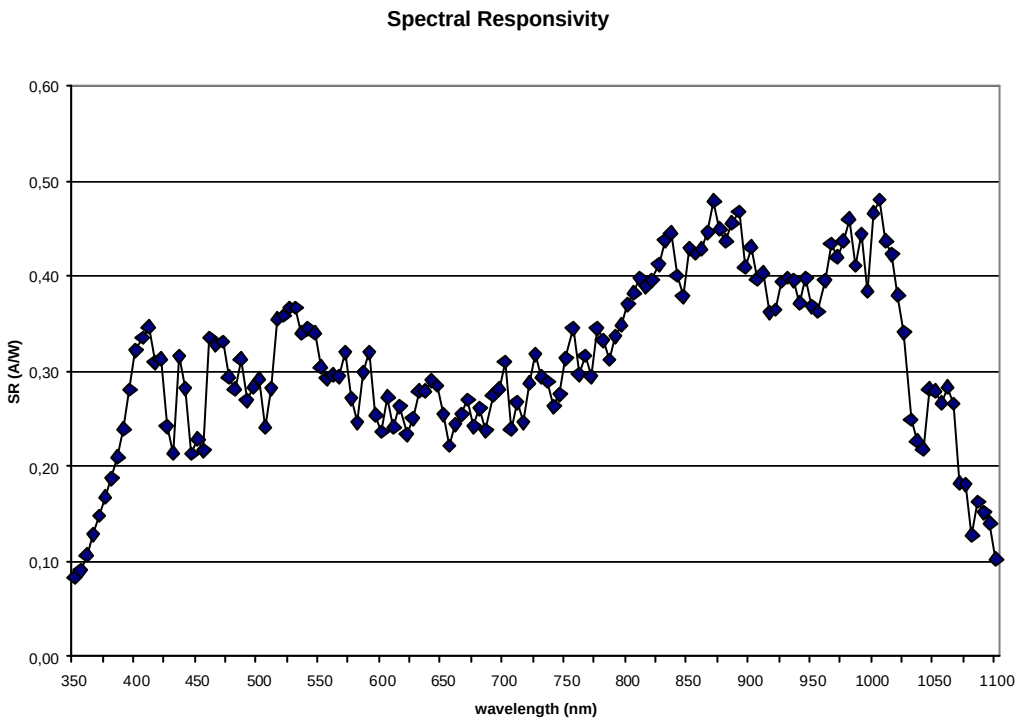
The major drawback of the logarithmic sensor is the presence of a time-invariant noise in the images. The Fixed Pattern Noise is caused by the nonuniformity of the transistors characteristics. In particular, threshold voltage variations introduce a voltage offset characteristic of each pixel. The FPN noise is removed from the images by adding to each pixel the corresponding offset ($v \rightarrow v + offset$, where v is the raw pixel value and *offset* is the FPN correction corresponding to the pixel). In CLinkCam, the FPN suppression is performed by the FPGA in real time and it is transparent to the user. The camera is shipped with one default correction frame. However, the user can easily replace the default frame.

The analog to digital conversion of the pixel signal is regulated by two parameters: VRef and VBG. VRef, the reference voltage, sets the position of the digitalization interval that is converted into 1023 discrete values. VBG, the band gap voltage, influences the width of this digitalization interval. From the user's point of view, VRef and VBG are two 8-bit parameters with typical values around 100 that can be modified to increase of decrease the average luminosity and contrast sensitivity of the image. For more detailed information see the Pupilla Datasheet.

ELECTRO OPTICAL CHARACTERISTICS

Array resolution	640 x 480
Pixel pitch	8 µm x 8 µm
Fill factor	0.40
Array size	5.120 mm x 3.840 mm
ADC resolution	10 bit
Differential non-linearity	1/2 LSB
Integral non-linearity	1 LSB
Dark Current	6.45 fA @ 27°C (*)
Photodiode Peak Responsivity	0.48 A/W @ 870 nm
Pixel Output Voltage Slope	-90.85 mV/dec @ 670 nm - irradiance range from 0.1 W/m^2 to 100 W/m^2,@ 32°C
Pixel output thermal drift	2.0mV/°C - irradiance range from 0.01W/m^2 to 100 W/m^2 and temperature range from 32°C to 111°C
Sensitivity (white light)	< 1 mW/m^2 - corresponding to ~ 0.2 lux
Fixed-pattern noise	13.0 % r.m.s. over whole array - referred to one decade @ 1 W/m
	12.5 mV r.m.s. over whole array - measured at pixel output @ 1 W/m
Dynamic Range	120 dB
Missing / dead pixels	none

(*) Dark Current is intended as leakage current of the photodiode



4 FPGA: THE PUPILLA INTERFACE

A Xilinx *XC2S30-5TQ144 Spartan-II* controls data transfer from and to the sensor Pupilla. The operations currently implemented on the FPGA are pixel addressing, sensor regulation, subtraction of the fixed pattern noise, and management of the I/O lines. The FPGA is programmed every time the camera is powered up. A 12-bit Flash memory contains the data used by the FPGA for the fixed pattern noise correction. The Flash access time is 90 nsec (this implies that FPN correction on FPGA cannot be

performed with frequencies higher than ~10MHz).

- **Pixel addressing.** Pixels of the Pupilla sensor can be randomly accessed; this means that any subset of the 640x480 pixel sensor can be captured without the need to acquire the whole frame. With the current FPGA implementation any rectangular Region of Interest can be acquired in the progressive scan mode.
- **Sensor regulation.** The analog to digital conversion of the pixel signal is regulated by two parameters: Vref and VGap. These parameters can be modified via software using a set of functions described in the Programming Library.
- **Fixed pattern noise correction.** The FPGA implements the fixed pattern noise correction. The raw value of each pixel is corrected at frame rate using the offset values stored in the Flash memory.
- **Management of the I/O lines.** The three general-purpose optoisolated lines can be used for synchronized image acquisition and control of industrial devices

The description of FPGA functions and commands is contained in section 13. The commands described in the document allow a complete control of pixel addressing, sensor regulation, FPN correction, and I/O ports.

5 FIXED PATTERN NOISE REMOVAL

The Flash memory dedicated to the FPGA contains the default correction frame that is used for FPN subtraction. The operation performed by the FPGA for each pixel is *v -> v + offset*, where *v* is the raw pixel value and *offset* is the FPN correction corresponding to the pixel. The correction frame stored in the Flash can be changed using the following procedure

a. A full frame with uniform intensity over the whole field of view is acquired (e.g. the image of a white sheet of paper). The light intensity should be close to the working average light intensity.
b. The average intensity is computed, $\bar{v} = \frac{1}{N}\sum_{j=1}^{N} v_j$ where index $j=1,\ldots,N$ runs over the pixel array. The average intensity, $\bar{v}$, is considered as the "true" pixel value.
c. For each pixel the difference between the true value and the measured value is computed. This value is the pixel offset, i.e. $offset_j = \bar{v} - v_j$. The array of offsets forms the *correction frame.*
d. The *correction frame* is stored into the flash memory.

Acquisition, computation and storage of the correction frame can be performed automatically using the software routine included in the sample program for image acquisition (see section 9). This routine uses the FPN correction commands described in Section 13.2.

6 THE CAMERA LINK INTERFACE: FACTS

CameraLink is a communication interface specifically designed for machine vision applications. It provides a standard communication protocol between cameras and frame grabbers, and offers high transfer rate and reliability. Five LVDS pairs compose the connecting cable, four for the data and one for the clock. The bandwidth can reach up to 2.38 Gbits/sec, more than enough for current needs. Camera Link supports asynchronous serial (RS232) communication to/from the camera from/to the frame grabber. Serial communication is generally used to regulate camera parameters. Camera Link does not support power requirements. Power to the camera has to be supplied by another cable.

7 I/O LINES

ClinkCam supports three optoisolated I/O lines. Looking at the back panel of the camera, six ports can be seen on the left side |6|5|4|3|2|1|. The pair (6,5) is the input line. The other two pairs, (4,3) and (2,1), are the output lines. The positive pole is on the right-hand side, i.e. (-, +). Current flowing through the ports should be less than 10 mA.

8 CLINKCAM CHARACTERISTICS

Box dimensions: width: 50 mm; height: 40 mm; depth 90 mm;
Sensor type: NeuriCam Pupilla 640x480 pixels, 10-bit pixel depth
I/O interfaces: CamerLink, 3 optoisolated I/O line: one input, and two outputs;
Lens: CS mount
Voltage range: from 8V to 16 V
Power consumption: 110 mA @ 9V;
Power on is signalled by a red LED.

9 GETTING STARTED

This section provides step-by-step instructions for the software installation. It is intended for the Euresys GrabLink frame grabber. Use Euresys Drivers MultiCam 2.6. The configuration files for the Neuricam CLink camera are contained in the included CD.
Open the CD. It contains:

1. The CLink camera configuration files in Folder Neuricam.
2. A sample program for image visualization in Folder AreaGrab
3. The included dlls are Borland Builder 5 dlls necessary to run the software (put them in the same directory of the .exe).
4. Folder Codice contains some functions necessary to compile the AreaGrab code (put this folder in C:/NeuriCam)
5. This document (User Manual)

9.1 CLINK CAMERA: INSTRUCTIONS

1) Install Euresys Drivers for the GrabLink Value frame grabber
2) Copy the camera configuration folder "Neuricam" in the **C:/Multicam/Cameras** directory
3) Copy the ***CLinkGrab*** folder in a chosen directory
4) Connect and power on ClinkCam: the power LED should be ON.
5) Run **AreaGrab.exe**
6) Click successively on
7) Channel -> Create -> GrabLink Board -> Neuricam -> ClinkCam -> Single Channel 10 Bit, Sync operation
8) (or Channel -> Create -> GrabLink Board -> Neuricam -> ClinkCam_line_scan -> Single Channel 10 Bit,
9) Sync operation)
10) Three Forms will appear: A) ***Image Display***, B) ***Controls***, and C) ***Histograms***
11) Click on ***Connect*** in form ***Controls***
12) Click on ***Initialize Camera*** in form ***Controls***
13) Click on ***Play*** button to visualize images

14) Click on ***Stop*** to end acquisition.

9.2 NOTE ON IMAGE VISUALIZATION

Images are captured with a 10-bit resolution. Since only 8 bits can be displayed on the screen, the program automatically selects a 256 gray-level region centred at the average value of the image histogram. This window can be manually centred using the slide bar on the ***Controls*** form.

9.3 NOTE ON SENSOR PARAMETERS

Two parameters regulate voltage digitalisation:

i) ***Vref*** regulates the ADC reference voltage. It has to be chosen so that the image histogram is well centred in the [0,1023] range. Normal operating values are between 90 and 110.

ii) ***Vgap*** regulates the quantization window, i.e. the voltage interval that it is quantized into 1024 levels. Normal operating values are between 90 and 110.

9.4 NOTE ON FIXED PATTERN NOISE REMOVAL

The Fixed Pattern Noise can be removed by FPGA or via software. The ClinkCam interface allows the user to redefine the correction frame and to download it into the Flash memory. Alternatively, the host PC can acquire raw images and FPN correction is performed via software.

9.5 FORM DESCRIPTION

A) Image Display Form

From left to right:

- Snap shot
- Live (Continuos image acquisition)
- Stop (Stop image acquisition)
- Capture background (for software fixed pattern noise removal)
- Reset background (set software correction frame to zero)
- Capture background, prepare correction frame and download it into the FPGA (the procedure is described in 13.4.2)
- Reset background for FPGA (set correction frame to zero)
- Triggered image acquisition
- Save currenct image as Windows Bitmap Image (8 bit for each pixel)
- Save current image (16 bit for each pixel)
- Compute egdes of acquired images
- Record N successive frame (the output files *.seq can be visualized using the program Pupilla Viewer)
- Use internal FPN (fixed pattern noise correction on FPGA)

B) Controls form

- Connect camera
- Initialise camera
- Choose the serial port dedicated to Camera Link

Image Control panel: from left to right and from top to bottom:

- Manual centring of the 8-bit visualization window.
- View image histograms (before and after fixed pattern noise removal) in real time
- Set Sensor Parameters (Vref, Vgap)

Debug Control panel: these commands regard the writing of the correction frame on the FPGA. This procedure is automatically executed using button Capture background in the ***Image Display Form.***

C) Histograms

- Image histograms (before and after fixed pattern noise removal) are displayed.

Mean value and standard deviation are shown.

10 SOURCE CODE

The source code of the visualization program xGrab is included in the CD. It was written using Borland Builder 5. If you want to modify it, use Builder 5 or superior. To recompile the code you need some NeuriCam classes contained in folder Codice. This folder should be put in the directory C:/Neuricam/.

The most importants files of the projects are *pupilla_commands.h* and *pupilla_commands.cpp***.** In these files the *ClinkCamControl* class is defined. The class manages serial communication with the camera. Configuration parameters, described in the tables showed below, are defined as constants in the *pupilla_commands.h.* The ClinkCamControl class can be used separately from the PupGrab software and it is a sample of the correct use of the commands.

11 REGION OF INTEREST

Since the Pupilla sensor supports random addressing, the FPGA can be programmed to acquire any subset of the whole frame. Rectangular ROI can be defined using a set of command described in section 12.1. By default, the ROI in thevisualization program AreaGrab is 640x480 pixels.
Changes of the ROI size (e.g. one line scan) can be performed by setting the appropriate parameters (number of rows, number of columns, start row, and start column)

1. in the camera configuration file contained in the C:/Multicam/Cameras/Neuricam directory,
2. in file ***pupilla.h*** in directory ***clink***
3. in files pupilla_commands.h and pupilla_commands.cpp in directory ***clink.***

The CMOS sensor Pupilla can be addressed randomly (as a memory). The pixel rate is 8MHz
The clock mounted in the camera is 16MHz and the sensor works at 8MHz. The corresponding frame rate is 24 f/s for a full frame (640x480).

12 DEFAULT PARAMETERS

The default parameters are

- Vref = 100
- Vgap=100
- ROI = 640x480
- Sensor frequency = 8 MHz

- Serial line baude rate = 9600bps

13 CAMERA CONTROL COMMANDS

The CameraLink interface provides (virtual) serial channels that can be used to send control commands to the camera. From the software point of view, the serial port is identical to a standard port (com1, com2, etc). Therefore, it is possible to take advantage of the standard Windows library to operate the serial port.

In the CLinkCam system serial communication is set to 9600bps for a 16MHz clock. If the camera clock is changed to 32MHz the baud rate should be increased to 19200 bps.

The ClinkCam control commands are organized into two categories: 1) Acquisition Commands, and 2) Fixed Pattern Noise Correction Setup commands.

13.1 ACQUISITION COMMANDS

Commands are listed and described in Table1. ***Name*** is the constant used in the c++ code to identify the communication command. Column ***Data*** indicates if the command has to be followed by a byte of data. For example, CLINK_SET_VREF sets Vref to the value specified by the following byte.

Table 1: commands list for the serial port.

Name	***Hex***	***Data***	***Description***
CLINK_START_SERIAL_COMM	0xBC		Enables communication. It has to be sent before any other command.
CLINK_STOP_SERIAL_COMM	0x00		Disables communication.
CLINK_GET_FPGA_ID	0x01		Not used
CLINK_LED_ON	0x02		Not used.
CLINK_LED_OFF	0x03		Not used.
CLINK_SET_DAC2_ADDR_01	0x04	1	Not used.
CLINK_SET_DAC2_ADDR_10	0x05	1	Not used.
CLINK_SET_DAC2_ADDR_00	0x06	1	Not used.
CLINK_SET_DAC2_ADDR_11	0x07	1	Not used.
CLINK_SET_VREF	0x08	1	Sets Vref (dac 1, addr 00)
CLINK_SET_VPREC	0x09	1	Sets Vprec(dac 1, addr 01)
CLINK_SET_VCM	0x0A	1	Sets Vcm(dac 1, addr 10)
CLINK_SET_VBG	0x0B	1	Sets Vbg(dac 1, addr 11)
CLINK_SET_CLK_PRESC	0x0C	1	Not used.
CLINK_ACQ_START_COL_ADDR_LOW	0x0D	1	Sets the low byte of the start column address (Cs)
CLINK_ACQ_START_COL_ADDR_HI	0x0E	1	Sets the high byte (aligned to the right) of the start column address (Cs)
CLINK_ACQ_STOP_COL_ADDR_LOW	0x0F	1	Sets the low byte of the end column address (Ce>Cs)

CLINK_ACQ_STOP_COL_ADDR_HI	0x10	1	Sets the high byte (aligned to the right) of the end column address (Ce>Cs)
CLINK_ACQ_START_ROW_ADDR_LOW	0x11	1	Sets the low byte of the start row address (Rs)
CLINK_ACQ_START_ROW_ADDR_HI	0x12	1	Sets the high byte (aligned to the right) of the start row address (Rs)
CLINK_ACQ_STOP_ROW_ADDR_LOW	0x13	1	Sets the low byte of the end row address (Re > Rs)
CLINK_ACQ_STOP_ROW_ADDR_HI	0x14	1	Sets the high byte (aligned to the right) of the end row address (Re>Rs)
CLINK_ACQ_SET_CONTROL_WORD	0x15	1	Sets the following - Bit 7 -> Pup_precenan - Bit 6 -> Pup_precena (not used) - Bit 5 -> Pup_precdisn (cfr. datasheet) - Bit 4 -> Pup_enaall (cfr. datasheet) - Bit 3 -> serializer_pwdn (cfr. datasheet serializer)
CLINK_ACQ_GET_SINGLE_FRAME	0x16		Captures a single frame
CLINK_ACQ_SET_INTERFRAME_TIME	0x17	1	Sets delay between the acquisition of two successive frames
CLINK_ACQ_ENABLE_CONTINUOUS	0x18		Sets continuous acquisition mode
CLINK_ACQ_DISABLE_CONTINUOUS	0x19		Stops acquisition
CLINK_ACQ_ENABLE_TRIG_CC1	0x1A		Not used
CLINK_NOT_USED1	0x1B		Not used
CLINK_NOT_USED2	0x1C		Not used
CLINK_NOT_USED3	0x1D		Not used
CLINK_NOT_USED4	0x1E		Not used

13.2 GENERAL PURPOSE OUTPUTS AND TRIGGERED ACQUISITION COMMANDS

Name	***Hex***	***Data***	***Description***
CLINK_CPO1_SET	0x31		Put hi the first the General Purpose Output (GPO1)
CLINK_CPO1_RESET	0x32		Put low GPO1
CLINK_CPO2_SET	0x33		Put hi GPO2
CLINK_CPO2_RESET	0x34		Put low GPO2
CLINK_ENABLE_EXT_TRIG	0x40		Start triggered acquisition
CLINK_DISABLE_EXT_TRIG	0x4f		Stop triggered acquisition

13.2.1 TRIGGERED ACQUISITION SETUP

The procedure to start triggered acquisition is:

1. Stop the grabber and sleep about ½ sec.
2. send CLINK_ACQ_DISABLE_CONTINUOUS.

3. send CLINK_ENABLE_EXT_TRIG to enable triggered acquisition.
4. wait until the camera acquires at least one frame.
5. start the grabber

To disable triggered acquisition:
1. stop the grabber
2. send CLINK_DISABLE_EXT_TRIG, the camera is stopped, to re-start acquisition send CLINK_ACQ_ENABLE_CONTINUOUS or start triggered acquisition.

13.3 FIXED PATTERN NOISE CORRECTION SETUP COMMANDS

The Fixed Patter Noise correction is regulated by the commands listed in Table 2. These commands
1. Perform writing of the Flash;
2. Must follow a well-defined procedure. On the contrary, acquisition commands can be sent at any time and order.

Table 2 : commands for the "FPN correction".

Name	***Hex***	***Data***	***Description***
CLINK_FLASH_ENABLE_WR	0x20		Sets ClinkCam into the flash writing mode
CLINK_FLASH_DISABLE_WR	0x21		Ends the flash writing mode
CLINK_FLASH_ERASE	---		Not used
CLINK_FLASH_RESET_POINTER	0x22		Reset the Flash Start Address (FLASH_PTR)
CLINK_FLASH_WR_BYTE_LO	0x23	1	Writes the least significant byte to address FLASH_PTR
CLINK_FLASH_WR_BYTE_HI	0x24	1	Writes the most significant byte to address FLASH_PTR
CLINK_ENABLE_FPN_CORRECTION	0x25		Enables run-time FPN correction
CLINK_DISABLE_FPN_CORRECTION	0x26		Disables run-time FPN correction
CLINK_FLASH_RD_WORD	0x27		Not used

13.4 FPN SETUP

The FPN correction procedure requires three steps
1. Clear the flash content (prepare the flash for writing)
2. Restart the camera.
3. Preparation of the correction frame
4. Download of the correction frame into the Flash
5. Enabling the “on-board fpn-correction”

13.4.1 PREPARATION OF THE CORRECTION FRAME

The preparation of the correction frame requires the acquisition of a background image and the computation of the offset for each pixel.
1. Acquire a background image (or average on several image)
2. Compute the correction frame as explained in section 5.

3. Each flash location is a 12-bit word. Offsets are 10-bit values. The bits not used should be set to one before downloading the correction frame.

13.4.2 DOWNLOADING THE CORRECTION FRAME ON FLASH

1. Enable serial communication: send command CLINK_START_SERIAL_COMM
2. Stop acquisition: send command CLINK_ACQ_DISABLE_CONTINUOUS
3. Pause for at least one second (the camera must complete the last acquisition sequence)
4. Disable FPN correction: send command CLINK_DISABLE_FPN_CORRECTION
5. Set ClinkCam in the Flash programming mode: send command CLINK_FLASH_RESET_POINTER
6. Start correction frame downloading. Each 16-bit location of the Flash requires the transfer of two bytes
    a. Write CLINK_FLASH_WR_BYTE_LO followed by the less significative byte
    b. Write CLINK_FLASH_WR_BYTE_HI followed by the most significative byte
    c. Repeat the procedure 640x480 times

   The FLASH_PTR pointer is incremented after each write operation
7. Close the writing session: send command CLINK_FLASH_DIABLE_WR

Note. The download (via serial line) requires 5 minutes approximatively.

13.4.3 ENABLE FPN CORRECTION

The command sequence to enable the FPN correction is:

1. stop acquisition
2. send CLINK_ENABLE_FPN_CORRECTION that enables the FPGA Fixed Pattern Noise correction
3. restart acquisition.

Command CLINK_DISABLE_FPN_CORRECTION disable internal fixed pattern noise correction.

14 TECHNICAL SUPPORT

For installation assistance or further information call NeuriCam at +39 0461 260552 or send an email message to techsupport@neuricam.com