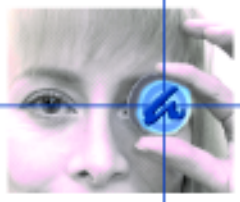

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Fast-VIDEO4 Board

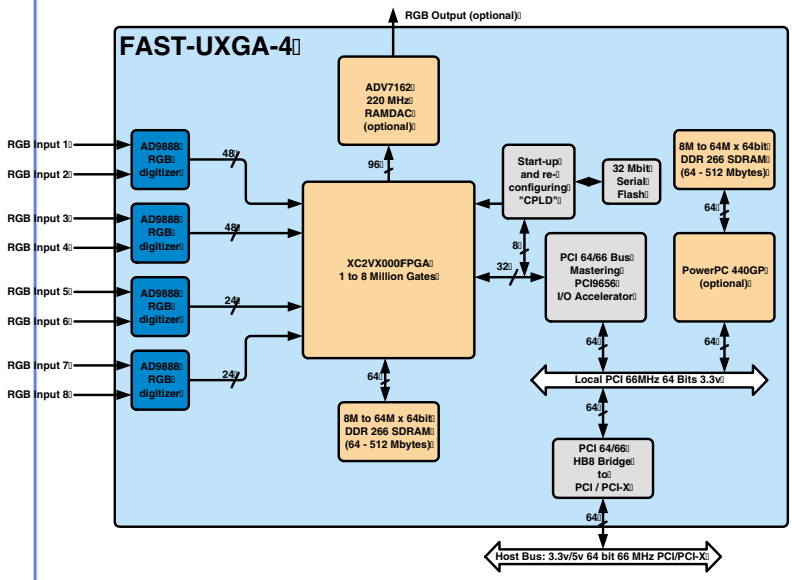
The Fast-VIDEO4 is the highest performance frame grabber for analog signals. The board is capable of simultaneously digitizing four independent UXGA sources without multiplexing and eight with multiplexing. The data can be processed in real-time using the large Xilinx FPGA of one to eight million gates or the 440GP PowerPC processor. The output can either be an optional UXGA display RAMDAC and/or the PCI-X bus.

Hardware, Software, Applications, and Systems for Machine Vision and Imaging

FUNCTIONAL UNITS:

- UXGA input X4
- Large programmable FPGA
- UXGA output (optional)
- 440GP PowerPC processor (optional)
- PCI-X interface

The major programmable units are the FPGA and the 440GP/PCI-X interface DMA engine.



BLOCK DIAGRAM OF THE HARDWARE

The hardware consists of a PCI raw form-factor PCI-X interface board with the following major functional units as shown in the diagram to the left

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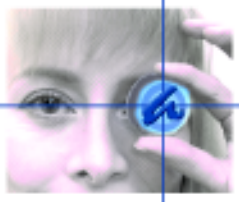
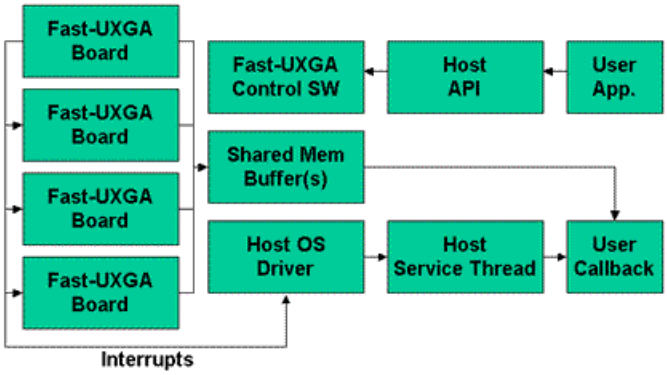
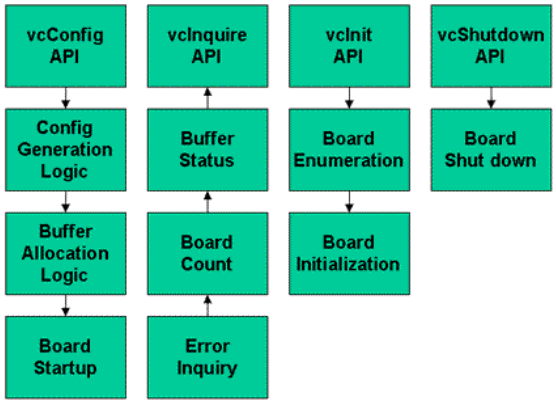


Fast-VIDEO4 Board

API Structure



API Diagram



Overview

The API provides configuration and control access to one or more FAST-UXGA boards. There is no specific limitation to the number of boards the software can support, though the number of slots in the computer imposes a practical limit.

The API supports enumeration of the boards, and the creation of "configurations', which determine the settings for all the boards in the system.

Multiple configurations can be defined, and then later selected by a single API call. This provides for switching modes as quickly as the hardware supports, typically one frame time for synchronized video, two frame times for asynchronous input video.

The API supports up to 8 configurations, which are delineated by the ConfigNumber field in the structures used to define a configuration. A particular configuration number applies across all the boards.

Combined image data is the DMA-ed into host memory by the PLX-9656 on each board. The DMA is a two dimensional DMA, in that a stride , offset, number of columns, and number of rows is provided in the hardware for each DMA. This allows images from multiple boards to be combined in memory into a large image, by re-using a buffer number across multiple boards in a configuration.

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